LOS ANGELES COUNTY DEPARTMENT OF PUBLIC WORKS TRAFFIC SIGNAL CONTROL EQUIPMENT SPECIFICATIONS

FEBRUARY 28, 2006

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CHAPTER 1 GENERAL REQUIREMENTS FOR TRAFFIC SIGNAL CONTROL EQUIPMENT

Section 1 SCOPE

1.1.1 **PRECEDENCE OF SPECIFICATIONS**: In case of conflict, the PLAN and DRAWINGS shall govern over CHAPTER 1, GENERAL REQUIREMENTS. All other individual chapters shall govern over the PLANS and DRAWINGS.

1.1.2 This Chapter defines the general requirements applicable to all equipment specified in this document. The intent of this specification is to establish the minimum acceptable electrical, mechanical, design, and performance requirements within which all equipment must operate satisfactorily and reliably. All items supplied shall be new and unused.

1.1.3 ALL equipment shall exist on the Los Angeles County -- Department of Public Works "QUALIFIED PRODUCT LIST" current at the time the equipment is furnished to the County.

1.1.4 Text:

Black Text	Normal Text
~~Strikethrough Text~~	Deleted Test
Red Underlined Text	New Text
Red Italic Underlined Text	***Temporary note***

Section 2 GLOSSARY

1.2.1 Wherever the following terms or abbreviations are used, the intent and meaning shall be interpreted as follows:

μ	Micro
μA	Microampere
μF	Microfarad
μH	Microhenry
μsec	Microsecond
A	Ampere
AC-	120 Volts AC, 60 Hertz grounded return to the power source.
AC	Alternating Current
AC+	120 Volts AC, 60 Hertz ungrounded power source.
ACIA	Asynchronous Communications Interface Adapter Device (Motorola MC6850 or equal).
AGENCY	Purchasing Government Agency. See COUNTY below.
AlInGaP	Aluminum Indium Gallium Phosphide Technology and material used in the production of the LED.
ANSI	American National Standards Institute
ASCII	American Standard Code for Information Interchange
Assembly	A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules.
ASTM	American Society for Testing and Materials
ATC	Advanced Transportation Controller
AWG	American Wire Gage
C Language	The ANSI C Programming Language
C	Celsius
Cabinet	An outdoor enclosure for housing the controller unit and associated equipment.
Cd	Candela, A unit of measurement of light intensity.
Certificate of Compliance	A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications.
Channel	An information path from a discrete input to a discrete output.
Chromaticity	The property of color of light
CIA	CMS Controller Isolation Assembly
CIP	CMS Interface Panel
CMOS	Complementary Metal Oxide Semiconductor
CMS SYSTEM	Includes Controller Unit, Model 334C Cabinet, Interconnect Harnesses, CMS and other associated equipment required to

	operate the system.
CMS	Changeable Message Sign
Component	Any electrical or electronic device.
Conflict Monitor	A device used to prevent conflicting green phases in conjunction with a controller (see TEES).
Contractor	The person or persons, manufacturer, firm, partnership, corporation, vendor, or combination thereof, which have entered into a contract with the COUNTY, as party or parties of the second part or his or their legal representative.
Controller Unit	A Traffic Signal Controller that is standard equipment on County maintained signalized intersections. In addition, That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly.
County	County of Los Angeles; specifically, the Director of Public Works, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them.
CPDA	CMS Pixel Driver Assembly
CPDM	CMS Pixel Driver Module
CPMM	CMS Pixel Matrix Module
CPU	Central Processing Unit (Note: also see MPU)
CR	ACIA Control Register
CRC	Cyclic Redundancy Check
DAT Program	Caltrans Diagnostic and Acceptance Test Program
Daughterboard	A printed circuit auxiliary interface board
dB	Decibel
dBa	Decibels above reference noise, adjusted.
DC	Direct Current
Device	Conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device. Interpretation shall be in the judgment of the Engineer
DIN	Deutsche Industrie Norm
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DTA	Down Time Accumulator
EEPROM	Electrically Erasable, Programmable, Read Only Memory Device
EG	Equipment Ground
EIA	Electronic Industries Association
EMI	Electro Magnetic Interference

Engineer	The Director of Public Works, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them.
EPROM	Ultraviolet Erasable Programmable Read Only Memory Device
Equal	Connectors: complying with physical dimensions, contact/pin material, plating and method of connection.
	Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device
ETL	Electrical Testing Laboratories, Inc
Firmware	A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM
FLASH Memory	A +5 VDC powered IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features
FPA	Front Panel Assembly
GaN	Gallium nitride material used in the production of the LED.
HEX	Hexadecimal
Hz	Hertz
I.D.	Identification
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IMP	Integrated Multi-protocol Processor
IRQ	Interrupt Request
ISO	International Standards Organization
ITE	Institute of Traffic Engineers
Jumper	A means of connecting/disconnecting two or more conductive points by soldering/desoldering a conductive wire jumper.
KB	Kilobytes
Laboratory	The established laboratory of the County or other laboratories authorized by the County to test materials involved in the contract
LED	Light Emitting Diode
Load switch	Series of devices used to switch power to signal indicators
LOGIC	Negative Logic Convention (Ground True) State
lsb	Least Significant Bit
LSB	Least Significant Byte
lx	Lux
m	Milli
M/170	Program Module /Model 170E Controller Unit Connector

M/170E	Caltrans, Model 170E Auxiliary Board Connector
mA	Milliampere
MB	Mega Byte
MCU	Micro Controller Unit (i.e.: MC68HC11)
METS	Material Engineering and Testing Services of the Translab.
MIC	Hitachi HD6303X microprocessor device (or equal) [for CALTRANS]
MIL	Military Specifications
MODEM	Modulation/Demodulation Unit
Module	A functional unit that plugs into an assembly
MOS	Metal Oxide Semiconductor
Motherboard	A printed circuit connector interface board with no active or passive components
MOV	Metal Oxide Varistor
MPU	Microprocessor Unit (Note: also see CPU)
MS	Military Standards
msb	Most Significant Bit
MSB	Most Significant Byte
msec	Millisecond
MUTCD	Manual on Uniform Traffic Control Devices
mW	Milliwatt
n	Nano
N	Newton (SI unit of force)
N.A., N/A	Presently not assigned, Cannot be used by the contractor for other purposes
N.C.	Normally closed contact
N.O.	Normally open contact
NEMA	National Electrical Manufacturers Association
nlsb	Next Least Significant Bit
NLSB	Next Least Significant Byte
NMI	Non-Maskable Interrupt
nmsb	Next Most Significant Bit
NMSB	Next Most Significant Byte
nsec	Nanosecond
PAL/PLA	Programmable Array Logic Device
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PDA	Power Distribution Assembly

Power Conditions	The level, hysteresis, and times, specified in the Controller Unit's specification.
Power factor	The ratio of the real power component to the total (complex) power component.
Power Failure	A Power Failure is said to have occurred when the incoming line voltage falls below the level and times specified in the Controller Unit's specification (2.1.2 below).
Power Restoration	Power is restored when the incoming line voltage equals the level and times specified in the Controller Unit's specification (2.1.3 below).
ppm	Parts per million
PTCSH	Pedestrian Traffic Control Signal Head
PV	Programmable Visibility Head. A traffic signal indication that can be "programmed" to limit the visible area of the indication.
PWM	Pulse Width Modulation
R/W	Model 170E Controller Unit Read/Write Control Line
RAM	Random Access Memory Device
Rated Power	The power consumption that the module was designed and tested for, at ambient temperature (25°C or 77°F). See Design Qualification Testing (1.4.1.9 below).
RDR	ACIA Receive Data Register
RES	Reset Interrupt
RF	Radio Frequency
RMS	Root-Mean-Square
ROM	Read Only Memory Device
ROT	Restart Orientation Timer
RTC	The Controller Unit Real Time Clock. This circuitry provides a CPU IRQ interrupt pulse (16.67 msec) clocked off the line frequency.
RTCA	Real Time Clock Adjuster Circuitry
RTS	Request To Send
S	Logic State
s	second
SCC	Serial Communication Controller
SCI	Serial Communications Interface
SDLC	Synchronous Data Link Control
Second Sourced	Produced by more than one manufacturer
SI	International System of Units
SMC	Serial Management Controller
SP	Serial Port (Switchpack when used in Tables B-2 and B-3)

SR	ACIA Status Register
SRAM	Static Random Access Memory Device
STATE	State of California
SW	Switch
TB, TBK	Terminal Block
TDR	ACIA Transmit Data Register
TEES	Traffic Electrical Equipment Specifications. A package of standard specifications for traffic electrical equipment to be used on State Highways. Caltrans Traffic Operations Program prepares this document.
THD	Total Harmonic Distortion. The amount of higher frequency power on the power line.
TOD	Time Of Day Clock
Triac	Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit
TSD No.1	8-32 SOUTHCO #47-62-301-20 or equal.
TSD No.2	8-32 SOUTHCO #47-62-301-60 or equal.
TSD No.3	M3 SOUTHCO #47-82-101-10 or equal.
TSD, (Thumb Screw Device)	A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No.2 shall be flat black.)
TSCES	Traffic Signal Control Equipment Specifications. A package of standard specifications for traffic electrical equipment. Los Angeles County Department of Public Works prepares this document.
TTL	Transistor-Transistor Logic
Type 1 module	A LED module designed to be mounted in the place of the existing lens of a traffic signal.
Type 2 module	A LED module designed to be mounted in the place of the incandescent lamp of a traffic signal utilizing the existing lens and lamp socket.
UL	Underwriter's Laboratories, Inc.
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VMA	Valid Memory Address
VME	Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
VTCSH	Vehicle Traffic Control Signal Head
Watchdog-Timer, (WDT),	A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts
x	Number Value
XX	Manufacturer's option

Figure 1-1: GLOSSARY

Section 3 GENERAL

1.3.1 All equipment furnished under these specifications shall be of solid-state design. Use of vacuum or gaseous tubes or electro-mechanical devices within the equipment is not acceptable unless otherwise indicated.

1.3.2 Los Angeles County reserves the right to bid any and all components when deemed in the best interests of the County, and/or where State or Federal participation requires that such components be purchased on a competitive bid basis.

1.3.3 **CODE REQUIREMENTS**: Traffic controls, parts, and accessories MUST meet the following codes wherever applicable:

Radio Manufacturers Association
National Electrical Code
Manual of Uniform Traffic Control Devices
ANSI Code.
NEMA
ASTM
ASA
Federal
State of California
Los Angeles County

1.3.3.1 In the event of conflict, the Los Angeles County Department of Public Works Standard Specifications for Public Works Construction, latest edition (and addenda) shall prevail.

1.3.3.2 Reference is made to CHAPTER 1SECTION 1 ABOVE(SCOPE). The County remains the sole judge on the ability of each device to meet specifications.

1.3.4 **DOCUMENTATION**:

1.3.4.1 Two manuals shall be supplied with each item required under this specification. Each controller cabinet assembly shall include two copies of the latest manual for each item of equipment that is furnished with the cabinet and enclosed in the shipping container. The county, at its option, may reduce the number of manuals required on a project.

1.3.4.2 Manual text font shall be Helvetica Bold, Gothic Legal 12, or equivalent. Text characters shall be no more than 10 characters per 25.4 mm and 7 lines per 25.4 mm, with the exception of schematic text, which shall be no more than 18 characters per 25.4 mm and 11 lines per 25.4 mm. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic, and shall suffer no degradation when subjected to normal cabinet temperature testing as described in this specification. The manual shall be printed on 215.9 mm by 279.4 mm (8.5 by 11 inch) paper, with the exception that schematics, layouts, parts lists and plan details may be on 279.4 mm by 431.8 mm (11 by 17 inch) sheets, with each sheet neatly folded to 215.9 mm by 279.4 mm (8.5 by 11 inch) size.

1.3.4.3 Each manual shall include the following parts in the order listed:

1. Table of Contents
2. Glossary
3. General Description
4. General Characteristics
5. Installation
6. Adjustments
7. Theory of Operation
   a. Systems Description (include block diagram).
   b. Detailed Description of Circuit Operation.
8. Maintenance
   a. Preventive Maintenance
   b. Trouble Analysis
   c. Trouble Shooting Sequence Chart
   d. Wave Forms
   e. Voltage Measurements
   f. Alignment Procedures
9. Technical Information: in the form of Manufacturer's published data sheets for medium and large scale integrated circuits.
10. Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).
11. Electrical Interconnection Details & Drawings
12. Schematic and Logic Diagram.
13. Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.

1.3.4.3.1 The date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals.

1.3.4.4 Prior to final printing, three copies of a preliminary draft of all manuals shall be submitted to the County for approval.

1.3.4.5 Updated documentation shall be provided for ANY and ALL design changes or modifications to equipment, circuits, or components supplied to the County. Notification of impending changes shall be made by letter, with support documentation to follow in an expeditious manner. Sufficient copies of documentation shall be provided at a rate of 10 copies total, or 1 copy for every 10 units supplied, whichever is greater.

1.3.5 **SAMPLE UNITS AND ACCEPTANCE TESTING**

1.3.5.1 Sample units may be complete Controller and Cabinet assemblies, or component parts. Sample units shall reflect all requirements contained in these Specifications. Final authority over the acceptance of sample units shall reside with the County of Los Angeles.

1.3.5.2 **PURCHASE AGREEMENTS**: Prior to bid acceptance, a complete sample unit, as specified by the County, shall be delivered to the County testing facility for acceptance testing.

1.3.5.2.1 Satisfactory completion of acceptance testing will be a prerequisite to formal acceptance of the Vendor's bid.

1.3.5.2.2 Rejection of the sample unit during acceptance testing will be grounds for rejection of the Vendor's bid, and the Vendor shall be responsible for removal of all rejected equipment from the County testing facility.

1.3.5.2.3 The County at its option may set aside the accepted sample unit, for the duration of the contract period, to ensure the consistency of supplied equipment. Changes to supplied equipment without prior County approval could result in rejection of non-accepted equipment. It is the Vendor's responsibility to supply only County accepted equipment, in order to avoid incurring delays or penalties.

1.3.5.2.4 The County reserves the right, at any time during the term of the contract, to reject any piece of equipment that fails to meet testing requirements or specifications. It is the Vendor's responsibility to rectify all discrepancies, and re-submit sample units as required for acceptance testing.

1.3.5.2.5 The County at its option, may, return all affected equipment, including warehoused equipment, to the Vendor for full credit, or exchange for newly acceptance-tested units.

1.3.5.2.6 Any and all expenses incurred, as a result of equipment being rejected during the term of the contract, shall be borne by the Vendor, including any penalties resulting from project delays.

1.3.5.3 **CASH CONTRACT projects, or TESTING AND INSPECTIONS for other agencies**:

CONTACT: Los Angeles County, Department of Public Works
Electrical Unit Head
1525 Alcazar Street
Los Angeles, CA 90033
CROSS ST: Soto Street, ½ mi. North of San Bernardino Freeway (I-10) [Thomas Guide map page 635-B2, formerly 45-B2]
PHONE: (626) 458-1708

1.3.5.3.1 **SCHEMATICS**: 30 days prior to inspection and testing, the contractor shall submit wiring schematics of controller cabinets to the above County testing facility for approval.

1.3.5.3.2 **TESTING**: Arrangements for inspection and testing by the County must be made in **ADVANCE.** Upon authorization, controller units, auxiliary equipment and/or wired cabinets, including manuals and approved wiring diagrams, shall be delivered to the County testing facility above.

1.3.5.3.2.1 The Contractor shall be directly responsible for reimbursement to the County of all costs incurred by the County for equipment testing. Upon delivery of equipment requiring testing, arrangements shall be made with the Electrical Unit Head for an initial testing deposit and final balance payment for the County incurred costs following equipment testing. The bid for the estimated cost of equipment testing shall be reflected in the bid for that item.

1.3.5.3.3 For **EACH CABINET** required for the project, the contractor shall allow 10 working days for inspection and testing, not to begin until **ALL EQUIPMENT** for said cabinet is delivered to the testing facility. The contractor shall contact the testing facility to obtain test results. It shall be the contractor's responsibility to pick up and deliver acceptable equipment to and from the testing facility.

1.3.5.3.4 The contractor shall remove all equipment submitted to the testing facility within 5 working days after notification of the test results. In the event the equipment is not removed within said period, it may be shipped to the contractor at his expense. It shall be the contractor's responsibility to pick up and deliver acceptable equipment to the project site.

1.3.5.3.5 Should any of the equipment fail to comply with the specifications, the contractor shall correct the deficiency and resubmit the equipment for an additional 10 working-day test period. All testing subsequent to rejection of the equipment, for failure to comply with specification requirements, will be at the expense of the contractor.

1.3.5.4 An appropriate Controller Diagnostic Test Program and Cabinet Verification Test Program shall be provided with sample controllers. One complete set of connectors and cables, wired per these specifications, shall be provided for use with the Diagnostic Test Programs.

1.3.5.5 Three (3) copies of a user's manual shall be provided. The User's Manual shall describe operation of all components included in the Sample Unit.

1.3.5.6 Four (4) sets of cabinet wiring diagrams shall be provided with the Sample Unit. Detailed equipment layout scale drawings and wiring diagrams of all equipment installed in the cabinet shall be submitted for approval prior to production.

1.3.6 **INTERCHANGEABILITY**: The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

ASSEMBLIES	ASSOCIATED DEVICES
Output File #1 & #2	Model 200 Load Switch Model 210P/210E Monitor Unit Model 2010 Monitor Unit Model 430 Heavy Duty Relay
Auxiliary Output File	Model 200 Load Switch Model 430 Heavy Duty Relay
Input File	Models 222, 224, 228, 232 Detectors Models 242, 252 Isolators
Power Distribution Assembly, PDA-1	Model 204 Flasher Unit Model 430 Heavy Duty Relay
Power Distribution Assembly, PDA-2	Model 204 Flasher Unit Model 206 Power Supply
Model 170E Controller Unit	Cabinet Models 332, 336, & 337 Model 400 MODEM Model 412F Memory Module 170E Input PCBA 170E Output PCBA
Model 170E-ATC Controller Unit	Cabinet Models 332, 336, 337 Model 170E HC11 MCU PCBA Model 400 MODEM Model 170E-ATC CHASSIS 170E Input PCBA 170E Output PCBA
Model 2070 Controller Unit	Model 2070-1 CPU Module Model 2070-2A and 2B Field I/O Module Model 2070-3 Front Panel Assembly Model 2070-4 Power Supply Model 2070-5 VME Cage Assembly Model 2070-6 Serial Comm. Module Model 2070-7A and 7B Serial Comm. Module
Cabinet Models 332, & 336	Model 170E Controller Unit Model 170E-ATC Controller Unit Model 2070 Controller Unit Input File Power Distribution Assembly #2 Output File #1 Auxiliary Output File

Figure 1-2: ASSEMBLIES and ASSOCIATED DEVICES

1.3.7 **INDICATORS AND CHARACTER DISPLAYS**

1.3.7.1 All indicators and character displays shall have a +45 degrees cone of visibility with its axis perpendicular to the front panel. All indicators and character displays shall be readily visible at a radius of up to 4 feet within the cone of visibility when the indicator is subjected to 9,000 foot-candles (97,000 lx) of white light with the light source at 45 (±2) degrees to the front panel. If characters are not self-luminous, illumination shall be provided for viewing in low levels of ambient light.

1.3.7.2 Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15 degrees minimum shall be provided for models 210P, 222, 228, 232, 242, 252, as well as a clearance of 30 degrees minimum for Models 200 and 204.

1.3.7.3 All indicators and character displays shall have a rated life of 100,000 hours minimum.

1.3.7.4 Liquid Crystal Displays (LCD) shall operate at temperatures of -34 degrees to 73 degrees Celsius without loss of visibility or bleeding. LCD's shall be back-lighted.

1.3.8 **CONNECTORS:**

1.3.8.1 **GENERAL:**

1.3.8.2 All connectors shall be keyed to prevent improper insertion of the wrong connector or PCBA.

1.3.8.3 The Contractor shall list the part number of the extraction tool recommended by its manufacturer.

1.3.8.4 TYPE T Connector shall be a single row, 10 position feed through terminal block. The terminal block shall be a barrier type with 6-32, 0.25 inch (6.35 mm), or longer, nickel-plated brass binder head screws. Each terminal shall be permanently identified as to its function.

1.3.8.5 The mating connectors shall be designated as the connector number and male/female relationship such as C1P (plug or PCBA edge connector) and C1S (socket).

1.3.8.6 The Type 25 connector shall be a 25 contact AMP HDP-20 connector (or equal) with gold on nickel-plated contacts. The female mating connector with socket contacts is designated Type 25S and the male mating connector with pin contacts is designated Type 25P. The Type 25P connector shall be provided with lock spring clips for latching to its mating connector.

1.3.8.7 PLASTIC CIRCULAR and M TYPE CONNECTORS **(C1, C2, C20, C30, C40, C4, C5, and C6)**

1.3.8.7.1 Pin and socket contacts for Connectors C1, C2, C20, C30, C40, C4, C5, and C6 shall be beryllium copper construction sub plated with 0.00005-inch (0.00127 mm) nickel and plated with 0.00003-inch (1.57 mm) gold. Pin diameter shall be 0.062 inch. Connectors shall have the following number of contacts:

C1: 104 contacts
C2, C20, C30, C40: 14 contacts
C4- 37 contacts
C5 & C6: 24 contacts

1.3.8.7.2 All pin and socket connectors of C1, C2, C20, C30, C40, C4, C5, and C6 shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

1.3.8.7.3 Connector C1 and C2, C20, C30, and C40 blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 Megohms. The contacts shall be secured in the blocks with stainless steel springs.

1.3.8.7.4 Connector C1, C2, C20, C30, and C40 corner guides shall be stainless steel. The guide pins shall be 1.097 inches (27.9 mm) in length and the guide sockets 0.625 inch (15.9 mm) in length.

1.3.8.7.5 Connector C4, C5 and C6 shall be circular plastic type with quick connect/disconnect capability and thread assist, positive detent coupling. The connectors shall be UL listed Glass Filled Nylon, 94 V-1 Rated, heat stabilized, fire resistant.

1.3.8.8 **PCB CONNECTORS**

1.3.8.8.1 PCB edge connectors shall have bifurcated gold plated contacts.

1.3.8.8.2 The PCB connector shall meet or exceed the following:

Operating Voltage:	600 VAC (RMS) at sea level
Current Rating:	5 amperes
Insulation Resistance:	5,000 Megohms
Contact Material:	Copper alloy plated with 0.00005 inch (0.00127 mm) of nickel and 0.000015 inch (0.00038 mm) of gold
Insulation Material:	Diallyl Phthalate or Thermoplastic
Contact Resistance:	0.006 ohm maximum

1.3.8.8.3 The two-piece PCB connector shall meet or exceed the DIN 41612.

1.3.8.8.4 The PCB 22/44 Connector shall have 22 independent contacts per side, dual-sided with 0.156-inch (3.96 mm) contact centers.

1.3.8.8.5 The PCB 28/56 Connector shall have 28 independent contacts per side, dual-sided with 0.156-inch (3.96 mm) contact centers.

1.3.8.8.6 The PCB 36/72 Connector shall have 36 independent contacts per side, dual-sided with 0.1-inch (2.54 mm) contact centers.

1.3.8.8.7 The PCB 43/86 Connector shall have 43 independent contacts per side; dual sided with 2.54 mm (0.100 inch) contact centers.

1.3.8.9 **WIRE TERMINAL CONNECTORS:** Each wire terminal shall be solderless with PVC insulation and a heavy-duty short -locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type-crimping tool.

1.3.8.10 **FLAT CABLE CONNECTORS –**

1.3.8.10.1 Each flat cable connector shall be designed for use with 26 AWG cable.

1.3.8.10.2 Each flat cable shall have dual cantilevered phosphor bronze contacts plated with 508 nm of gold over 1270 nm of nickel.

1.3.8.10.3 Each flat cable shall have a current rating of 1 A minimum and an insulation resistance of 5 Megohms minimum.

1.3.8.11 **PCB HEADER POST CONNECTORS –**

1.3.8.11.1 Each PCB header post shall be 1.0 mm square by 8.7 mm high.

1.3.8.11.2 Each PCB header post shall be mounted on 4.0 mm centers.

1.3.8.11.3 Each PCB header post and shall be tempered hard brass plated with 381 nm of gold over 1.270 mm of nickel.

1.3.8.12 **PCB HEADER SOCKET CONNECTORS:**

1.3.8.12.1 Each PCB header socket block shall be nylon or diallyl phthalate.

1.3.8.12.2 Each PCB header socket contact shall be removable, but crimp-connected to its conductor.

1.3.8.12.3 Each PCB header socket contact shall be brass or phosphor bronze plated with 562 nm of gold over 1270 nm of nickel.

1.3.9 SURGE PROTECTION DEVICE: A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 amperes. It shall have the following ratings:

IMPULSE BREAKDOWN:	Less than 1,000 volts in less than 0.1 us at 10 KV/us
STANDBY CURRENT:	Less than 1 ma.
STRIKING VOLTAGE:	Greater than 212 volts

1.3.10 **PACKAGING**: Each item delivered shall be individually packed in its own shipping container. When loose Styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the Styrofoam.

1.3.11 **DELIVERY**: Each item delivered for testing shall be complete, including manuals, and ready for testing.

1.3.12 **METALS**

1.3.12.1 All sharp edges and corners shall be rounded.

1.3.12.2 All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

1.3.12.3 **ALUMINUM**

1.3.12.3.1 Sheet shall be Type 5052-H32 ASTM designation B209.

1.3.12.3.2 Rod, Bar and Extruded shall be Type 6061-T6, or equal.

1.3.12.4 **STAINLESS STEEL**

1.3.12.4.1 Sheet shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

1.3.12.5 **COLD ROLLED STEEL**

1.3.12.5.1 Sheet, Rod, Bar and Extruded shall be Type 1018/1020.

1.3.12.5.2 PLATING: All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class 1 or zinc plating meeting the requirements of (ASTM B633-85 Type II SC4, or) Federal Specification QQ-Z-325B, Type 2 Class 1.

Section 4 COMPONENTS

1.4.1 **GENERAL:**

All components shall be second sourced and shall be of such design, fabrication, nomenclature, or other identification as to be purchased from a wholesale electronics distributor, or from the component manufacturer, except as follows:

1.4.1.1 **Spare Components:** When a component is of such special design that it precludes the purchase of identical components from any wholesale electronics distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used. The County, at its option, may reduce the number required.

1.4.1.2 Circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

1.4.1.3 Only Memory and CPU devices shall be socket mounted on the PCBA. No other device shall be socket mounted unless specifically called out.

1.4.1.4 No component shall be operated 80% above its maximum rated voltage, current or power ratings. Digital components shall not be operated more than 3% above their nominal voltage, current, or power ratings.

1.4.1.5 No component shall be provided where the manufactured date is 2 years older than the contract award date. The design life of all components, operating for 24 hours a day operating in their circuit application, shall be 10 years or longer.

1.4.1.6 Where the potential for damage by shock or vibration exists, a clamp, fastener, retainer, or hold-down bracket shall support the component mechanically.

1.4.1.7 Except as specified in 1.4.1.8 below, all discrete components, such as resistors, capacitors, diodes, transistors, and integrated circuits shall be individually replaceable. Components shall be arranged so they are easily accessible for testing and maintenance.

1.4.1.8 Encapsulation of 2 or more discrete components into circuit modules is prohibited, except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators, Nov-RAM and transistor arrays.

1.4.1.9 The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

1.4.1.10 Within the circuit of any device, module, or PCBA, electrical isolation shall be provided between DC logic ground, equipment ground and the AC grounded (neutral) conductor. They shall be electrically isolated from each other by 500 Megohms, minimum, when tested at the input terminals with 500 VDC.

1.4.2 **CAPACITORS**

1.4.2.1 The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%.

1.4.2.2 A capacitor, which may be damaged by shock or vibration, shall be supported mechanically by a clamp or fastener.

1.4.2.3 Capacitor encasements shall be resistant to cracking, peeling, and discoloration.

1.4.2.4 All capacitors shall be insulated and shall be marked with their capacitance value and working voltage.

1.4.2.5 Electrolytic capacitors shall not be used for capacitance values of less than 1.0 Microfarad and shall be marked with polarity.

1.4.3 POTENTIOMETERS

1.4.3.1 Potentiometers with ratings from 1 to 2 watts shall be equivalent to Military Type RV4.

1.4.3.2 No potentiometers less than 1 watt rating shall be used (except for trimmer type function).

1.4.3.3 The power rating of any potentiometer shall be at least 100% greater than the maximum power requirements of the circuit.

1.4.3.4 All trimmer potentiometers shall have 10 turns minimum.

1.4.4 **RESISTORS**

1.4.4.1 Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications: MIL-R-11F or MIL-R-22684.

1.4.4.2 All resistors shall be insulated and shall be marked with their resistance value. Resistance values shall be indicated by the EIA color codes, or by stamped value (power resistors).

1.4.4.3 Resistor tolerance shall not exceed 5% of the indicated value.

1.4.4.4 The value of the resistors shall not vary by more than 5% between -37 degrees and 74 degrees Celsius.

1.4.4.5 Resistors that have a rating exceeding 2 watts shall not be used unless special ventilation or heat sinking is provided. They shall be insulated from the PCBA.

1.4.5 **SEMICONDUCTOR DEVICES**

1.4.5.1 All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.

1.4.5.2 All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

1.4.5.3 The pin "1" location of all sockets shall be properly marked on the PCBA adjacent to each socket.

1.4.5.4 **TRIACS** – Each Triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with a machine screw and nut with integral lock washer.

1.4.6 **TRANSFORMERS AND INDUCTORS**

1.4.6.1 All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or laminations.

1.4.6.2 All transformers and inductors shall have their windings insulated and shall be protected to exclude moisture.

1.4.6.3 All transformer and inductor leads shall be color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

1.4.7 **CIRCUIT BREAKERS** (10 amperes or greater)

1.4.7.1 Circuit breakers shall be listed by UL or ETL. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker. All circuit breakers (30 amperes or greater) shall be quick-break on either automatic or manual operation. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. An ambient air temperature range of from 18 degrees to 50 degrees Celsius shall not influence overload tripping. Minimum interrupting capacity shall be 5,000 amperes, RMS.

1.4.7.2 For circuit breakers 80 amperes and above, the minimum interrupting capacity shall be 10,000 amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carlingswitch Time Delay Curve #24 or equal). *(Note: added text from Caltrans specifications.)*

1.4.7.3 Circuit breakers shall be the trip-free type.

1.4.7.4 Multi-pole breakers shall be the common-trip type.

1.4.7.5 All Fuses shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the holder. Fuses shall be easily accessible and removable without use of tools.

1.4.8 **SWITCHES**

1.4.8.1 **DIP**: Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 mA, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 mA, 30

VDC. The contacts shall be gold over brass (or silver). The switch shall be rated for a minimum of 40,000 operations.

1.4.8.2 **LOGIC**: The switch contacts shall be rated for a minimum of one-ampere resistive load at 120 VAC or 28 VDC and shall be silver over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.4.8.3 **CONTROL**: The switch contacts shall be rated for a minimum of five-ampere resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.4.8.4 **POWER**: Ratings shall be the same as CONTROL except the contact rating shall be a minimum of ten amperes at 125 VAC.

1.4.9 **TERMINAL BLOCKS**: The terminal blocks shall be barrier type, rated at 20 amperes and 600 VAC RMS minimum. The terminal screws shall be 7.938 mm minimum length nickel-plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

1.4.10 WIRING, CABLING AND HARNESSES

1.4.10.1 **HARNESSES** shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize cross talk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements.

1.4.10.2 Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

1.4.10.3 Wiring shall be routed to prevent conductors from being in contact with metal edges. Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

1.4.10.4 All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

1.4.10.4.1 Conductor color identification shall be as follows:

Grounded AC circuits:	Gray or white
Equip. Ground:	Solid green or continuous green color with 1 or more yellow stripes
DC logic ground:	Continuous white with a red stripe.
Ungrounded AC+:	Continuous black or black with colored stripe
Signal or ungrounded DC logic:	Any color not specified

Section 5 MECHANICAL

1.5.1 **ASSEMBLIES AND PCBA DESIGN**

1.5.1.1 **ASSEMBLIES** (including Controller Unit): All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBA with the following exceptions (NOTE: The power supply for the controller shall be a plug-in assembly):

1.5.1.1.1 Motherboard and daughterboard assemblies.

1.5.1.2 Assemblies shall be provided with 2 guides for each plug-in PCBA or associated device (except relays). The guides shall extend to within 0.75 inch from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.5.1.3 **PRINTED CIRCUIT BOARDS**: Also refer to PRINTED CIRCUIT BOARDS CHAPTER 1Section 1 below. No components, traces, brackets, or obstructions shall be within 0.125 inch (3.175 mm) of the board edge (guide edges). Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.5.1.3.1 Lock Washers shall not come into direct contact with printed circuit boards. Flat washers must be added to prevent damage.

1.5.1.4 The Controller Unit shall be modular in design, and each module shall be easily removable with a minimum use of tools. All single-board modules shall be vertically mounted, including any combination of: CPU, I/O, voltage regulation, display, Modem, or Prom.

1.5.1.5 The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all items. Placement of this information for modules such as the Model 210P Monitor Unit, Model 400 MODEM, and Model 412 Program Module shall be on the PCBA.

1.5.2 **WORKMANSHIP**: Workmanship shall conform to the requirements of this specification and shall be in accordance with the highest industry standards.

1.5.3 **MODEL NUMBERS**

1.5.3.1 The manufacturer's model number, serial number and circuit issue or revision number shall appear on the rear panel of all equipment and modules supplied.

1.5.3.2 In addition to any assignment of model numbers by the manufacturer, a model number assigned in the Figure below shall be displayed on the front panel in bold type, at least 0.25 inch high.

MODEL	DEVICE
170E	Type 170E Controller Unit
170E-ATC	Type 170E-ATC Controller Unit
200	Load Switch
204	Flasher Unit
206	Power Supply Module
210P/210E	Type 210 Plus (/Enhanced) Monitor Unit
222	Two Channel Loop Sensor Unit
224	Four Channel Loop Sensor Unit
227	Magnetometer Sensor Element
228	Magnetometer Sensor Unit
231	Magnetic Element
232	Magnetic Sensor Unit
242	DC Isolator
252	AC Isolator
400	Modem
402	Support Assembly
412F	Memory Module
2010	Type 2010 Monitor Unit
2070	Type 2070 Controller Unit

Figure 1-3: MODEL NUMBERS

1.5.4 All PCBA connectors mounted on a motherboard or daughterboard shall be mechanically secured to the chassis or frame of the unit.

1.5.5 All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

1.5.6 **TOLERANCES**: The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal: ±1.334 mm (0.0525 inch)
Edge Guides: ±0.381 mm (0.015 inch)
PCBA: +0.254 mm (0.010 inch)

Section 6 ENGINEERING

1.6.1 **HUMAN ENGINEERING**

1.6.1.1 To the highest practicable degree, the unit shall be engineered for simplicity and ease of operation and maintenance. This shall include the following:

1.6.1.1.1 No more than two potentiometers, controls or switches may be mounted concentrically. Knobs for such devices shall have diameters in a ratio of 2:1 outer to inner. The outer knob shall have a diameter of at least 1 inch.

1.6.1.1.2 Knobs shall be of large enough diameter (at least 0.5 inch (12.7 mm) diameter) and of great enough separation (at least 0.5 inch (12.7 mm) edge to edge) to assure ease of adjustment without disturbance of adjacent knobs.

1.6.1.1.3 All fuses shall be easily accessible and shall be replaceable without the use of any tools.

1.6.1.1.4 PCBAs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCBA connectors.

1.6.1.1.5 PCBAs shall require a force no less than 5 pounds (22.24 N) or greater than 50 pounds (222.4 N) for insertion or removal.

1.6.2 **DESIGN ENGINEERING**

1.6.2.1 The following practices shall be employed in the design of solid state equipment circuitry:

1.6.2.2 The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range

1.6.2.3 For reasons of personal safety, personnel shall be protected from all dangerous voltages.

1.6.3 **GENERATED NOISE**: No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface

Section 7 PRINTED CIRCUIT BOARDS

1.7.1 **DESIGN, FABRICATION, AND MOUNTING**

1.7.1.1 No components, traces, brackets, or obstructions shall be within 0.125 inch (3.175 mm) of the board edge (guide edges).

1.7.1.2 Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.7.1.3 The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBAs.

1.7.1.4 All single-board modules shall be vertically mounted, including any combination of CPU, I/O, voltage regulation, display, Modem, or Prom.

1.7.1.5 All contacts on PCBAs shall be plated with a minimum thickness of 0.000030 inch (0.000763 mm) gold over a minimum thickness of 0.000075-inch (0.001905 mm) nickel.

1.7.1.6 PCBA design shall be such that components may be removed and replaced without damage to boards, traces, or tracks.

1.7.1.7 Fabrication of PCBAs shall be in compliance with Military Specification: MIL-P-13949, except as follows:

1.7.1.7.1 Only NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0626-inch (1.590 mm) minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 2 ounces per square foot (0.556 kilogram per square meter) with adequate cross section for current to be carried. All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper track. Jumper wires will not be permitted, except from plated-through padded holes to an external component or for designed function selection with the jumper insulated and as short as possible.

1.7.1.7.2 In Section 3.3 of Military Specification MIL-P-13949G Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better. Class of permissible bow or twist shall be Class C (Table V) or better. Class of permissible warp or twist shall be Class A (Table II) or better.

1.7.1.7.3 Sections 4.2 through 6.6 of Military Specification: MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.

1.7.1.8 The mounting of parts and assemblies on the PCBA shall conform to Military Specification MIL-STD-275E, except as follows:

1.7.1.8.1 All semiconductor devices required to dissipate more than 250 mW or any case temperature that is 10 degrees Celsius above ambient shall be mounted with spacers, transipads or heat sinks to prevent direct contact with the PCBA.

1.7.1.8.2 When completed, all residual flux shall be removed from the PCBA.

1.7.1.8.3 The resistance between any two isolated, independent conductor paths shall be at least 100 Megohms when a 500 VDC potential is applied.

1.7.1.8.4 All PCBAs shall be coated with a moisture resistant coating, after installation of components.

1.7.1.8.5 Where less than 0.25-inch (6.35 mm) lateral separation is provided between the PCBA (or the components of a PCBA) and any metal surface, a 0.03125 (-0.0 to 0.0156) inch (0.79375 +/-0.39624 mm) thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCBA.

1.7.1.9 Each PCBA connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be ... 0.045 ("0.005) inch for 0.1 inch spacing and 0.055 ("0.005) inch for 0.156 inch spacing (1.143 +/- 0.127 mm for 2.54 mm spacing and 1.40 +/- 0.127 mm for 3.96 mm).

1.7.2 **SOLDERING**

1.7.2.1 Hand soldering shall comply with Military Specification: MIL-P-55110.

1.7.2.2 Automatic flow soldering shall conform to the following conditions:

1.7.2.2.1 A Constant speed conveyor system.

1.7.2.2.2 Conveyor speed shall be the optimum to minimize solder peaks or points, which form at component terminals.

1.7.2.2.3 Temperature shall be controlled to within "8 degrees Celsius of the optimum temperature.

1.7.2.2.4 The soldering process shall result in the complete coverage of all copper runs, joints, and terminals with solder except that which is covered by an electroplating process.

1.7.2.2.5 Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

1.7.2.2.6 If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCBA after the flow process has been completed.

1.7.3 **DEFINITIONS**: Definitions for the purpose of this section on PCBAs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.

Section 8 QUALITY CONTROL

1.8.1 The following measures shall be taken by the Contractor during the production process to ensure a high standard of quality.

1.8.2 **COMPONENTS**: All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the unit.

1.8.3 **SUBASSEMBLIES OR MODULES**

1.8.3.1 Visual inspections shall be performed on all modules, printed circuits, and subassemblies to determine any physical defects such as cracking, scaling, poor fastening, incorrect component values, etc.

1.8.3.2 Complete electrical testing shall be performed on each module, printed circuit or subassembly to determine its compliance with the manufacturer's design function.

1.8.3.3 Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence.

1.8.4 UNITS

1.8.4.1 The completely assembled unit shall be subjected to a full environmental cycling and timing test.

1.8.4.2 The unit shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

1.8.5 **PRE-DELIVERY REPAIR**

1.8.5.1 The procedures listed below shall be followed in repair of equipment before shipment.

1.8.5.1.1 Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

1.8.5.1.2 Defects in PCBAs or electronic circuit components shall be specially treated as follows:

1.8.5.1.3 A PCBA may be flow soldered a second time if copper runs and joints are not satisfactorily coated on the first run.

1.8.5.1.4 Under no circumstances shall a PCBA be flow soldered more than twice.

1.8.5.1.5 Hand soldering may be used for printed circuit repair.

Section 9 ELECTRICAL, ENVIRONMENTAL, and TESTING

1.9.1 **GENERAL**

1.9.1.1 The General procedures and equipment used in the evaluation of the controller unit, cabinet, and auxiliary equipment are a minimum guide and should not limit the testing and inspection to ensure compliance of the equipment with these specifications.

1.9.1.2 **CERTIFICATION:** The Contractor who shall certify that he has conducted inspection and testing in accordance with these specifications. See “CONTRACTOR'S TESTING CERTIFICATION” below.

1.9.2 **INSPECTION**: A visual and physical inspection shall include mechanical, dimensional, and assembly conformance of all parts of these specifications that can be checked visually or manually with simple measuring devices.

1.9.3 **ENVIRONMENTAL:** All components shall properly operate within the following limits:

1.9.3.1 Ambient Temperature: -37 degrees to 74 degrees Celsius

1.9.3.2 Humidity: 5 to 95 percent, from 1.1 Degrees C to 46.0 Degrees C.

1.9.3.3 The relative humidity and ambient temperature values in the following Figure shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY AT BAROMETRIC PRESSURES (29.92 In. Hg.)		
Ambient Temperature/ Dry Bulb (in degree C)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in degree C)
-37.0 to 1.1	10	-17.2 to 42.7
1.1 to 46.0	95	42.7
48.8	70	42.7
54.4	50	42.7
60.0	38	42.7
65.4	28	42.7
71.2	21	42.7
74	18	42.7

Figure 1-1 TEMPERATURE vs. HUMIDITY

1.9.3.4 **SHOCK TEST**: Test per Specification MIL-STD-810E Method 516.4.

1.9.3.5 **VIBRATION TEST**: Test per Military Specification MIL-STD-810E Method 514.4, equipment class G (Common Carrier).

1.9.3.6 Cabinets shall comply with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment".

1.9.3.7 All equipment shall continue normal operation when subjected to the following:

1.9.3.7.1 **LOW TEMPERATURE TEST:** With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be lowered from 20 degrees Celsius to –37 degrees Celsius at a rate of not more than 18 degrees Celsius per hour. The item shall be cycled at -37 degrees Celsius for a minimum of 5 hours and then returned to 20 degrees Celsius at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.9.3.7.2 **HIGH TEMPERATURE TEST:** With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be raised from 20 degrees Celsius to 70 degrees Celsius at a rate of not more than 18 degrees Celsius per hour. The item shall be cycled at 70 degrees Celsius for a minimum of 5 hours and then returned to 20 degrees Celsius at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.9.4 **ELECTRICAL:** All components shall operate properly within the following limits:

1.9.4.1 Applied Line Voltage: 90 to 135 VAC

1.9.4.1.1 All circuits unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 VAC to 90 VAC at a rate of 2 ("0.5) volts per second.

1.9.4.2 Frequency: 60 ("3.0) Hertz

1.9.4.3 All equipment, when housed within its associated cabinet, shall be unaffected by transient voltages normally experienced on commercial power lines. Equipment purchased separately from the cabinet will be tested for compliance with the equipment housed within a County accepted Model 332 cabinet and the cabinet connected to the commercial power lines.

1.9.4.3.1 The power line surge protection (including the cabinet protection and that internal to the equipment) shall enable the equipment under test to withstand (nondestructive) and continue to operate normally following exposure to test signals (applied at the Cabinet Service Terminal Block). The test signals shall comply with ANSI/IEEE C62.41 (100kHz. Ring Wave, the 1.2/50us-8/20 Combination Wave and the EFT Burst) at voltages and currents specified at "Location Category B2" and "Test Severity" level III (i.e. up to 4.0 kV, open-circuit).

1.9.4.3.1.1 The EFT Burst test signal will be applied for 10 minutes. The Ring Wave and Combination Wave will each be applied at a rate of once every 10 seconds for a maximum for 50 occurrences per test.

1.9.4.3.1.2 The unit under test will be operated at 20 degrees "5) Celsius and at 120 ("12) VAC.

1.9.4.3.1.3 The controller unit communications modules shall be tested resident in a County -accepted controller unit, which in turn is housed in a County-accepted cabinet.

1.9.4.3.2 EQUIPMENT PURCHASED SEPARATELY FROM THE CABINET:~~.~~ Equipment that may be purchased separately from the cabinet shall also be tested for compliance as follows:

1.9.4.3.2.1 Power from commercial power lines applied at Cabinet Service Terminal Block

1.9.4.3.2.2 Equipment properly housed and connected within a County Accepted Model 332 Cabinet

1.9.4.3.2.3 The Cabinet Power Surge Protectors deactivated or removed

1.9.4.3.2.4 The power line surge protection (including the Cabinet protection and that internal to the equipment) shall enable the equipment under test to withstand (nondestructive) and continue to operate normally following exposure to test signals (applied at the Cabinet Service Block). The test signals shall be in compliance with ANSI /IEEE C62.41 (100kHz. Ring Wave, and the EFT Burst) at voltages and currents specified at "Location Category A1" (i.e. up to 2.0 kV, 0.07 kA for the 100kHz Ring Wave) and at up to "Test Severity" level I (i.e. up to 1.0 kV open-circuit) for the EFT Burst.

1.9.4.3.2.5 The EFT Burst test signal will be applied for 10 minutes. The Ring Wave will be applied at a rate of once every 10 seconds for a maximum for 50 occurrences per test.

1.9.4.3.2.6 The unit under test will be operated at 20 degrees (" 5) Celsius and at 120 ("12) VAC.

1.9.4.3.2.7 The controller unit communications modules shall be tested resident in a County -accepted controller unit, which in turn is housed in the cabinet.

1.9.4.4 Within the circuit of any device, module or PCBA, electrical isolation shall be provided between DC logic ground, equipment ground and the AC grounded conductor. The DC logic ground and equipment ground shall be electrically isolated from the AC grounded conductor and from each other by 500 Megohms, minimum, when tested at the input terminals with 500 VDC.

1.9.4.5 All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage to the cabinet at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

1.9.4.6 All equipment shall resume normal operation following a period of at least 5 hours at -37 degrees Celsius, when 90 VAC is applied to the input terminals of the cabinet.

1.9.5 **MODEL 170E, 170E-ATC, and 2070 CONTROLLER DIAGNOSTIC TEST PROGRAM**

1.9.5.1 The Contractor shall furnish a Diagnostic Test Program, with the provided controller unit, at the time of delivery. The Program shall test and report failures on all functions and circuits within the controller. This Program shall meet the requirements in the Chapter of this specification for the Controller Model provided.

1.9.5.2 Five copies of a Diagnostic Test Program Software Manual shall be supplied. The Manual shall include full and complete documentation of test procedures, including, but not limited to the following:

Diagnostic Test Operation
Individual Diagnostic Tests
Program listings in Assembly Format, with detailed comments
Detailed Flow Charts, which are keyed to the software listing using instruction labels and subroutine names.

1.9.6 **CABINET VERIFICATION PROGRAM**

1.9.6.1 The Vendor shall furnish a Cabinet Verification Program, ~~resident in 27256 EPROM (s),~~ with each cabinet assembly unit, at the time of delivery. The program shall test cabinet wiring related to the Output File, Input File, police panel, and flash switches. In addition, the program shall check conflict monitor operation by generating all possible conflicts, in sequence, and resetting the monitor automatically. It shall also check all operational features of the supplied conflict monitor, whether specified or not.

1.9.6.2 Five copies of a Cabinet Verification Program Software Manual shall be supplied. The Manual shall include full and complete documentation of test procedures, including, but not limited to the following:

1.9.6.2.1 Cabinet Verification Test Operation

1.9.6.2.2 Individual Diagnostic Tests

1.9.6.2.3 Program listings in Assembly Format, with detailed comments

1.9.6.2.4 Detailed Flow Charts, which are keyed to the software listing using instruction labels and subroutine names.

1.9.7 **CONTRACTOR'S TESTING CERTIFICATION**

1.9.7.1 The Contractor shall supply, with each shipment, a full test report of the quality control and final test conducted on each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

1.9.7.2 The Contractor shall submit his quality control procedure and format of test reports to the County for approval within 15 days following the approval of the contract.

1.9.7.3 The QUALITY CONTROL procedure shall include the following:

1.9.7.3.1 Acceptance testing of all supplied components.

1.9.7.3.2 Physical and functional testing of all modules.

1.9.7.3.3 A minimum 100-hour burn-in of all modules.

1.9.7.3.4 Physical and functional testing of all items.

1.9.7.3.5 A minimum 24-hour operation of all controller units and cabinets.

1.9.8 **WARRANTIES AND GUARANTEES**

1.9.8.1 It is the responsibility of the Vendor to ensure that all equipment provided has been thoroughly tested prior to shipment, and that each shipment conforms to these specifications.

1.9.8.2 The minimum warranty for any equipment and materials shall be for a period of one (1) year from the date of test acceptance, or the date received by the County, whichever date is later. The warranty shall cover all manufacturer's defects, parts, labor, and shipping costs.

Section 10 CHAPTER DETAILS

1.10.1 SECTION NOTES:

1.10.2 All dimensions are in millimeters

1.10.2.1 M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 Megohms. The contacts shall be secured in the blocks with stainless steel springs.

1.10.2.2 M Type connector corner guides shall be stainless steel. The guide pins shall be 27.86 in length and the guide sockets shall be 15.66 in length.

1.10.2.3 Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated, heat stabilized and fire resistant.

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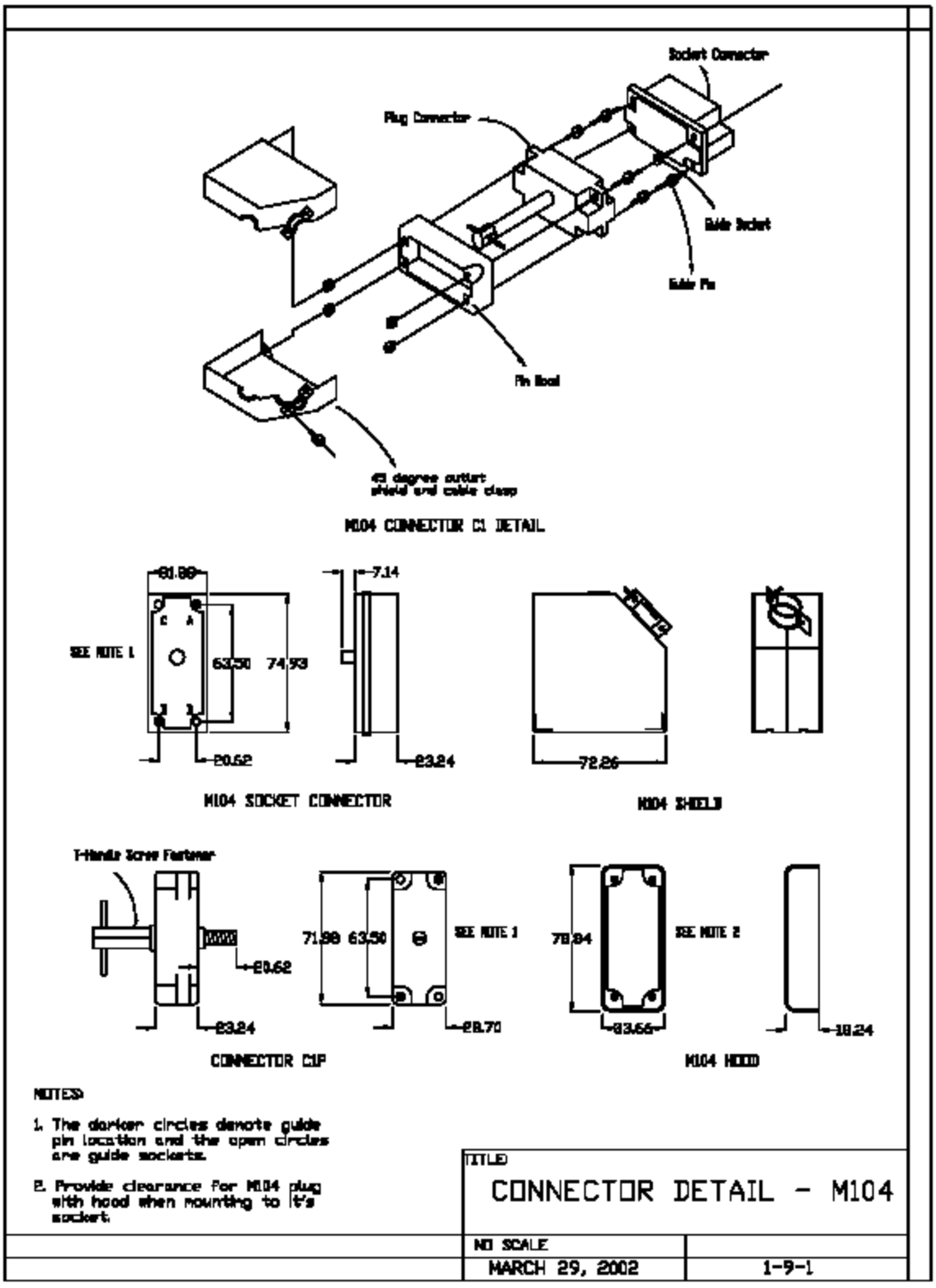


Figure 1-4: TEES DRAWING 1-9-1, CONNECTOR DETAIL - M104

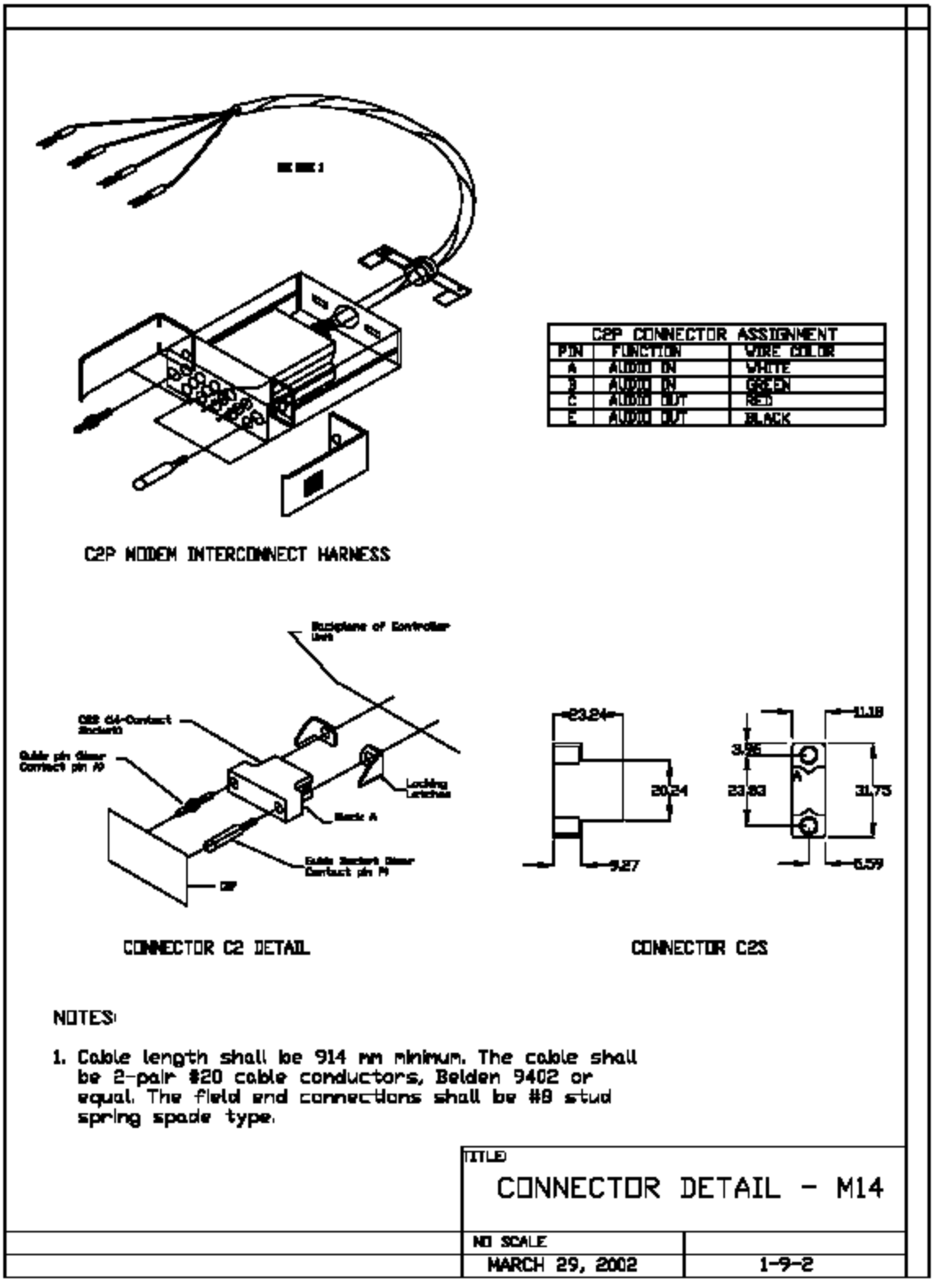


Figure 1-5 TEES DRAWING 1-9-2 Connector Detail - M14

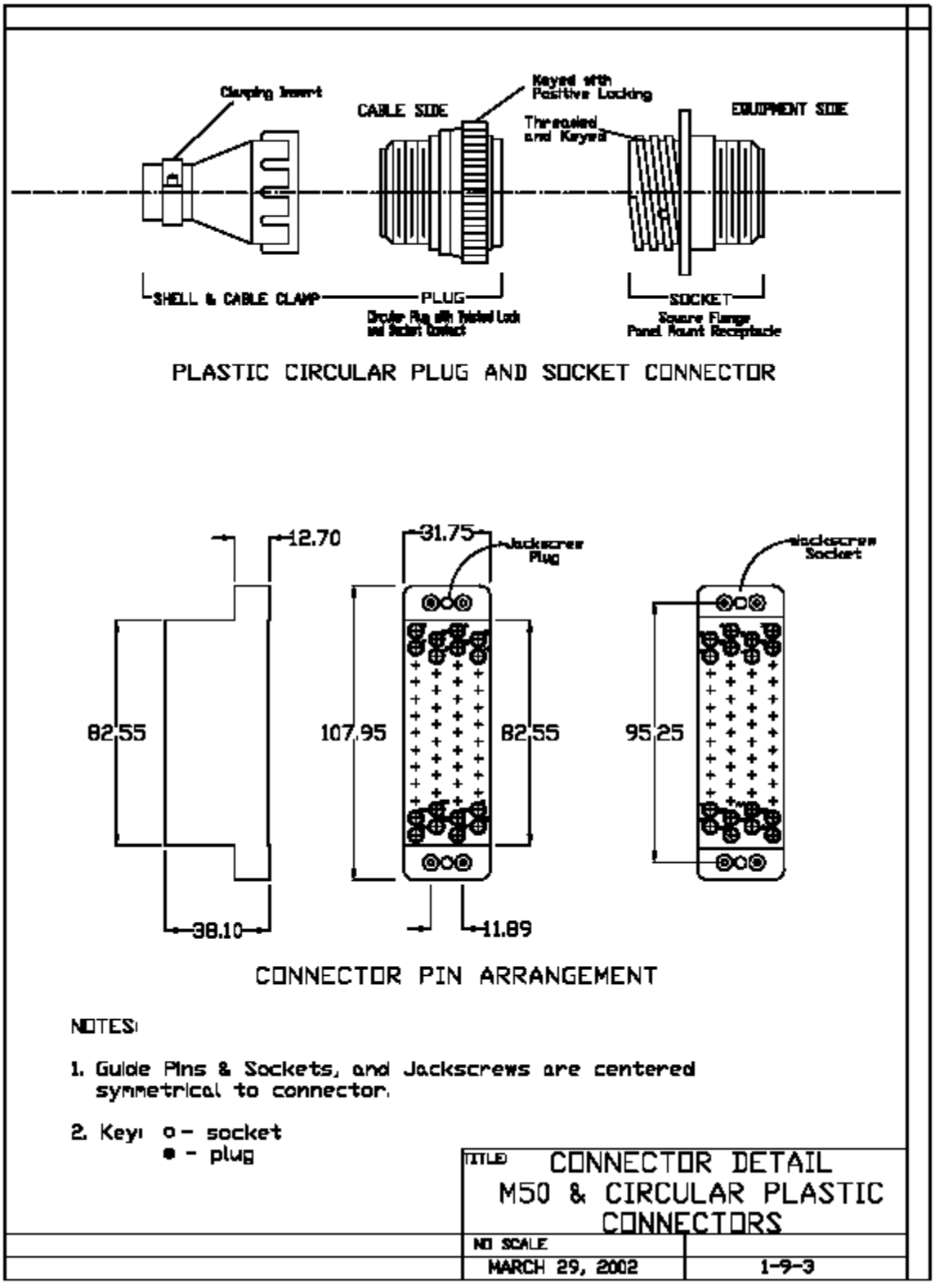


Figure 1-6 TEES DRAWING 1-9-3, Connector Detail M50 & Circular Plastic Connectors

CHAPTER 2 MODEL 170E CONTROLLER

Section 1 GENERAL

2.1.1 **170E Controller:**

2.1.1.1 The 170E was an upgrade of the original 170 Controller. The 170E was built to increase reliability and handle increased communication requirements.

2.1.1.2 It uses a type **6802** CPU, 32K NRAM (less I/O) and 32K EPROM program memory. The EPROM and NRAM is jumper configured to be on the CPU Board or on the Type 412 Memory Module. Communication is thru 4 ACIA Ports with two type 400 modem slots.

2.1.1.3 The 170E Chassis (see 2.3.2 below) and 6802 CPU PCBAs, HC11 MCU PCBAs and ATC-HC11 PCBAs, shall be compatible.

2.1.2 **POWER FAILURE**: A power failure is said to have occurred when the incoming line voltage falls below 92 "2) VAC for 50 msec. The determination of the 50 msec interval shall be completed within 67 msec of the time the voltage falls below 92 ("2) VAC.

2.1.3 **POWER RESTORATION**: Power is considered restored when the incoming line voltage equals or exceeds 97 ("2) VAC for 50 msec. The determination of the 50 msec interval shall be completed within 67 msec of the time the voltage first reaches ("2) VAC.

2.1.4 **POWER HYSTERESIS:** The hysteresis between power failure and power restoration voltage settings shall be a minimum of 5 volts and a maximum of 6 volts.

2.1.5 Each memory device shall stabilize to normal operation within 10 msec following Power Restoration and shall be in Standby until addressed.

2.1.6 All memory devices shall be second sourced and shall operate over the specified electrical and environmental ranges of the controller unit, and shall have access times at or below 200 nanoseconds.

2.1.7 **SPARE MODULES**: The manufacturer shall provide one complete set of replacement modules for every 100 controller-units purchased on a contract. One set of complete replacement modules is listed as following:

1. CPU/MPU Board
2. Input Board
3. Output Board
4. Display Board (if used)
5. Front Panel Board and Keypad (s)
6. Unit Power Supply
7. Any other circuit boards used.

2.1.8 **EPROM MEMORY**

2.1.8.1 The EPROM supplied with the 170E controller shall be ceramic INTEL 27C256A, or equivalent, hereafter referred to as "EPROM."

2.1.8.2 **RAM MEMORY**: All RAM supplied shall be Non-Volatile as described below, hereafter referred to as "NOV-RAM" or “NRAM”.

2.1.8.3 Each NOV-RAM device shall be mounted in a Memory Assembly. The Memory Assembly shall incorporate a self-contained Lithium energy source with control circuitry that automatically protects data during loss of power. RAM data retention shall be a minimum of 10 years from date of assembly manufacture.

2.1.8.4 Only Nov-RAM Memory Assemblies manufactured within the previous 12 months shall be delivered to the County. The month and year of manufacture, shall be clearly and permanently marked, on the top of the device.

2.1.8.5 NOV-RAM MEMORY devices supplied for the CPU Module shall be 32KByte DALLAS 1230Y IND, or equivalent.

2.1.8.6 NOV-RAM MEMORY devices supplied for the Memory Module shall be 32KByte DALLAS 1230Y IND, or equivalent.

2.1.8.7 NOV-RAM with REAL TIME CLOCK (optional), devices supplied for the ATC-HC11 MCU Module shall be a DALLAS DS1644, 32K byte NRAM with built in Real Time Clock, or equivalent.

2.1.9 The total READ/WRITE time including buffering, decoding, device access time and accessed data presented to the controller unit data bus shall not exceed 300 nsec for a 6802 CPU or 200 **0**sec for MC68HC11 MCU (approximately one fourth of the ECLK). Memory devices shall have read and write time suitable to perform either function in one CPU/MCU instruction cycle.

2.1.10 Socket mounting shall be provided **ONLY** for CPU, MCU, NRAM, and EPROM devices. Each CPU or NRAM socket shall have machined pins and gold-plated contacts, and shall have its component identification permanently marked on the PCBA adjacent to the socket. EPROM sockets shall be a "Zero Insertion Force" Type. Sockets shall be:

2.1.10.1 For NRAM Socket:

28 pins Augat 828-AG10D or equal

2.1.10.2 For EPROM Socket:

28 pins	BR Intec Garry ZIF #06-00084, 3M OEM ZIP DIP #228-1296-00-3303 or equal
32 pins	3M OEM ZIP DIP #232-1297-00-3303 or equal

2.1.10.3 For CPU/MCU Socket:

40 pins (6800 type CPU)	BR Intec Garry ZIF #06-00086, Augat 840-AG10D or equal
68 pin (MC68HC11F1 MCU)	AMP PLCC socket #821574-1 series HPT or equal

2.1.11 If a Programmable device is used for address decoding and timing algorithms, the device code listing together with data sheet (s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the contractor uses to directly reproduce the device.

2.1.12 All circuit boards shall be coated with an insulating compound as specified in MIL-I-46058C Amendment 6. The insulating material shall have a fluorescent tracer added to facilitate examination by ultraviolet illumination.

2.1.13 ALL devices and components used in the design of the controller shall meet the temperature and electrical specifications outlined in this specification.

2.1.14 Use of extender boards shall not interfere with normal controller unit operation.

Section 2 ELECTRICAL

2.2.1 A 3-conductor cable a minimum of 3 feet in length shall supply the AC power to the controller unit. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

2.2.2 The front panel and chassis shall be connected to equipment ground.

2.2.3 The controller unit shall be unaffected by transient voltages normally experienced on commercial power lines. Refer to 1.8.5.1.5 above (ELECTRICAL, ENVIRONMENTAL, AND TESTING).

2.2.3.1 At a minimum, Surge arrestors shall be provided between AC+, AC- and EG for protection against power line noise transients. The surge arrestors shall meet the following **minimum** requirements:

Recurrent peak voltage:	212 Volts
Energy rating maximum:	20 Joules
Power dissipation, average:	0.85 Watt
Peak current for pulses less than 6 Fsec:	2000 Amperes
Standby current:	Less than 1 mA

2.2.3.2 Two 0.5 ohm, 10 watt (**minimum**) wire-wound power resistors, shall be provided (1 on the AC+ power line and 1 on the AC line) for protection of the surge arrestors.

2.2.3.3 Input and emission suppression shall be provided, across the AC+ and AC- power lines, by a CorCom 3S1A device (**equivalent or better**).

Section 3 CHASSIS

2.3.1 **GENERAL**

2.3.1.1 The controller unit shall be designed to mount in a standard EIA 19inch rack. Maximum height shall not exceed 7 inches.

2.3.1.2 The controller unit shall be housed in a compact, portable aluminum enclosure suitably protected against corrosion.

2.3.1.3 A permanent mechanical means shall be provided for each plug-in board, or module, excluding the Memory Module, to prevent accidental loosening due to vibration or transportation.

2.3.1.4 All printed circuit board modules shall be easily removable from the front of the controller unit, without the use of tools or disassembly of the controller chassis

2.3.1.5 All circuit boards shall be vertically mounted.

2.3.1.6 **BOARD SPACING AND PLACEMENT**

2.3.1.6.1 Lateral spacing between boards shall be a minimum of 1.0 inch (25.4mm) from the PCBA surface to any component or surface of an adjacent board.

2.3.1.6.2 Continuous nylon card guides, with ejectors, shall be provided for all internal PCBAs. Card guides shall be securely bonded to the chassis.

2.3.2 **170E CHASSIS:**

2.3.2.1 The Memory Module and the Caltrans Option board shall be placed next to the CPU board, with lateral spacing (as defined in 2.3.1.6.1 above) not to exceed 1.5 inches (38.1mm).

2.3.2.2 Modem slots shall be placed between the CPU board and the I/O.

2.3.2.3 The depth placement of the vertical M/170 Connector shall be such that the Memory Module Front Panel shall be flush with the Model 170E Controller Unit Front Panel when the module is connected.

Section 4 CONNECTORS

2.4.1 **GENERAL**

2.4.1.1 All circuit board connectors shall be pin compatible from the 170E Chassis to the 170E-ATC Chassis.

2.4.1.2 Connector C1S shall be mounted to allow access from the rear of the controller unit, and provide 44 inputs and 56 outputs of control interface to and from external devices or files.

2.4.1.3 The Model 400 Modems and CPU ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (Type T Connector), mounted on the rear panel of the controller unit.

2.4.1.4 C2S, C20S, C30S, and C40S shall all be AMP 201298-1 sockets.

2.4.1.5 ACIA 1, 2, 3 & 4 / MODEM 1 and 2 shall have the following Pin Assignments (NOTE: All functions are in reference to a Modem's perspective):

SIGNAL	T-1, ACIA 1, MODEM 1	C2s, ACIA 1, MODEM 1	C20s, ACIA 2, MODEM 1	C30s, ACIA 3, MODEM 2	C40s, ACIA 4, MODEM 2
AUDIO IN	1.	A.	A.	A.	A.
AUDIO IN	2.	B.	B.	B.	B.
AUDIO OUT	8.	C.	C.	C.	C.
AUDIO OUT	9.	E.	E.	E.	E.
+5 VDC	N/A	D.	D.	D.	D.
CD	3.	H.	H.	H.	H.
RTS	4.	J.	J.	J.	J.
DATA IN	5.	K.	K.	K.	K.
DATA OUT	7.	L.	L.	L.	L.
CTS	6.	M.	M.	M.	M.
DC GND	10.	N.	N.	N.	N.
N.C.		F.	F.	F.	F.
N.C.		P.	P.	P.	P.
N.C.		R.	R.	R.	R.

Figure 2-1: ACIA/MODEM CONNECTORS

2.4.1.6 +5 VDC shall be the only power supply voltage available on these connectors, and it shall be derived from a separate voltage regulator. (See Section 5: Power Supply)

2.4.1.7 The maximum total current available to these connectors from the +5V power supply shall be limited to 300 mA.

2.4.1.8 A PCBA 22/44S Connector shall be provided for the Model 400 Modules and a PCBA 36/72S Connector shall be provided for the Memory Module and the Caltrans Option board.

2.4.1.9 Ribbon Cables, if used, shall terminate with properly rated and easily repairable connectors. Ribbon cables shall not terminate onto plug-in modules. If specialized tools are required to repair the supplied ribbon cables; two (2) sets of such tools shall be provided. The ribbon cables shall be dressed in a neat and orderly fashion to avoid sharp bends.

Section 5 POWER SUPPLIES

2.5.1 A power supply shall be provided to produce all DC power necessary to operate the controller unit. The power supply shall be modular and easily removable from the chassis.

2.5.2 Power Supply design shall be such that all components are operated at or below 80 percent of their maximum ratings.

2.5.3 Voltage regulators shall comply to the following specifications over a line voltage range of 90VAC to 135VAC:

REGULATION	CURRENT (MIN)	RIPPLE AND NOISE (MAX)
+ 5 ("0.10V) (Logic)	2.4A	100mV P-P
+ 5 ("0.25V) (C2, C20, C30, C40)	300mA	100mV P-P
+12 ("0.60V)	1.0A	100mV P-P
-12 ("0.60V)	500mA	100mV P-P
- 5 ("0.25V) required only if needed for the controller to operate.	400mA	100mV P-P

Figure 2-2: VOLTAGE REGULATION

2.5.4 If regulated +5V is required for the Display Module, a separate regulator shall be used.

2.5.5 Test points shall be provided for monitoring all power supply voltages. All test points shall be clearly labeled and readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 0.0625 inch (1.59mm) diameter and 0.1875 inch (4.76mm) high, minimum. The clearance between test points and other components shall be 0.25-inch (6.35mm), minimum.

2.5.6 The DC ground shall not be connected to equipment ground.

2.5.7 Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ("17) msec after the NMI line goes LOW.

2.5.8 The maximum DC voltage generated shall not exceed 45 volts.

2.5.9 The Power Supply shall be designed so that all required filtering and regulation be achieved within the power supply module.

2.5.10 **STANDBY POWER:** A stored-capacitance type device shall be provided in lieu of a battery. This device shall be used to power **ONLY** the Down Time Accumulator (DTA) circuit, and be of sufficient capacity to operate the DTA for a minimum of 8 hours, while the controller unit is powered down.

Section 6 MOTHERBOARD and BUS SYSTEM

2.6.1.1 All circuit boards shall be pin compatible from the 170E Chassis to the 170E-ATC Chassis.

2.6.2 **SYSTEM MEMORY MAP: Model 170E with 6802 CPU BOARD**

FUNCTION	ADDRESS RANGE	BYTES USED
CPU BOARD NRAM	0000 - 0FFF	4K
CPU NRAM (INT/EXT)	1000 - 4FFF	16K
DTA RESET (WRITE)	5000	1
DTA MINUTES (READ)	5000	--
RESTART ORIENTATION TIMER	5004	1
INPUT (READ)	5001 - 500A	10
OUTPUT (WRITE)	5001 - 500A	--
RESERVED	500B - 500E	4
DTA SECONDS (READ)	500F	1
RESERVED	5010 - 5FFE	4079
RTC RESET (WRITE)	5FFF	1
STATUS BYTE (READ)	5FFF	--
STATUS BIT 1: ACIA #1 IRQ	5FFF – 1	--
STATUS BIT 2: ACIA #2 IRQ	5FFF – 2	--
STATUS BIT 3: ACIA #3 IRQ	5FFF – 3	--
STATUS BIT 4: ACIA #4 IRQ	5FFF- 4	--
STATUS BIT 5: * spare	5FFF-5	--
STATUS BIT 6: * RESERVED	5FFF-6	--
STATUS BIT 7: DTA MAXOUT	5FFF-7	--
STATUS BIT 8: RTC IRQ	5FFF-8	--
ACIA #1	6000 – 6001	2
ACIA #2	6002 – 6003	2
ACIA #3	6004 – 6005	2
ACIA #4	6006 – 6007	2
RESERVED	6008 - 600F	8
CPU BOARD NRAM	6010 - 6FFF	4K
OPTION BOARD	7000 - 700F	16
MEMORY MODULE NRAM (INT/EXT)	7010 - 7FFF	4K
TRAFFIC SIGNAL EPROM (INT/EXT)	8000 – FFFF	32K

INT ONLY = Addresses reference a on the CPU board.
EXT ONLY = Addresses reference external from the CPU/MPU board.
INT/EXT = Two jumpers select whether the address ranges for these devices reference addresses internal to or external from the CPU/MPU board.
Pulled high (or set low using the ground true jumper option). Bit 6 is the Memory Map Configuration Status Bit.

Figure 2-3: 6802 SYSTEM MEMORY MAP

2.6.3 **SYSTEM MEMORY MAPS: 170E with optional Type ATC-HC11 MCU BORD:**

2.6.3.1 Reference: 170E-ATC SYSTEM MEMORY MAPS in Chapter 3 section 3.6.2

Figure 2-4: 68HC11 MEMORY BANKS

2.6.4 **I/O and CONTROL ADDRESS MAP: 170E with Type ATC-HC11 MCU BOARD**

2.6.4.1 Reference: 170E-ATC I/O and CONTROL ADDRESS MAP in Chapter 3 section 3.6.2

Figure 2-5: 68HC11 SYSTEM MEMORY MAP

2.6.4.2 68HC11 MCU CONFIG REGS and RAM.

FUNCTION	ADDRESS RANGE	BYTES USED
RESERVED	7000	1
68HC11 MCU REGISTERS	7001	1
68HC11 PORT G (BANK SWITCHING)	7002	1
68HC11 MCU REGISTERS	7003-7009	7
RESERVED	700A	1
68HC11 MCU REGISTERS	700B-705F	85
68HC11 MCU RAM (volatile)	7060-73FF	~1K

Figure 2-6: 68HC11 CONFIG REGS

2.6.5 **I/0 AND MEMORY SYSTEM BUSSES:** Two separate busses off the CPU board shall be provided: one for I/O, and one for the Memory system. All lines to the Memory Buss shall be Tri-State logic, and shall be in the high Impedance State when not in use, to allow the Memory Module to be inserted or removed with the 170E controller power ON.

2.6.6 **INPUT & OUTPUT INTERFACES** shall utilize ground-true logic. The transfer of data between interface and working registers within the CPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of CPU read/write command at the time the given address is valid.

2.6.6.1 **OUTPUT INTERFACE:** The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the CPU. This interface shall provide an open collector output capable of sinking up to 100 mA at 40 VDC. A "1" from the CPU shall be presented as a grounded collector, and a "0"' presented as an open circuit. Once a port is written, the data shall remain present and stable either until another word is written into it or until the power is turned off.

2.6.6.2 The state of these output ports at the time of power up, or below power failure threshold, shall be an open circuit.

2.6.6.3 **OUTPUT MAP**:

OUTPUT PORT	170E, 6802 CPU ADDRESS	170E, 68HC11 MCU ADDRESS	BIT	FUNCTION
1	5001	7401	1	C1 – 2
			2	C1 – 3
			3	C1 – 4
			4	C1 – 5
			5	C1 – 6
			6	C1 – 7
			7	C1 – 8
			8	C1 – 9
2	5002	7402	1	C1 – 10
			2	C1 – 11
			3	C1 – 12
			4	C1 – 13
			5	C1 – 14
			6	C1 – 15
			7	C1 – 16
			8	C1 – 17
3	5003	7403	1	C1 – 19
			2	C1 –20
			3	C1 – 21
			4	C1 – 22
			5	C1 – 23
			6	C1 – 24
			7	C1 – 25
			8	C1 – 26
4	5004	7404	1	C1 – 27
			2	C1 – 28
			3	C1 – 29
			4	C1 – 30
			5	C1 – 31
			6	C1 – 32
			7	C1 – 33
			8	C1 – 34
5	5005	7405	1	C1 – 35
			2	C1 – 36
			3	C1 – 37
			4	C1 – 38
			5	C1 – 100
			6	C1 – 101
			7	C1 – 102
			8	C1 – 103
6	5006	7406	1	C1 – 83
			2	C1 – 84
			3	C1 – 85
			4	C1 – 86
			5	C1 – 87
			6	C1 – 88
			7	C1 – 89
			8	C1 – 90
7	5007	7407	1	C1 – 91

			2	C1 – 93
			3	C1 – 94
			4	C1 – 95
			5	C1 – 96
			6	C1 – 97
			7	C1 – 98
			8	C1 – 99
8	5008	7408	1	Character control, Phase
			2	Character control, Interval
			3	Character control, Timing, LS
			4	Character control, Timing, NLS
			5	Character control, Timing, NMS
			6	Character control, Timing, MS
			7	Call Light 8
			8	Call Light 9
9	5009	7409	1	Character, LS
			2	Character, NLS
			3	Character, NMS
			4	Character, MS
			5	Decimal Point
			6	Blanking, Phase and Interval
			7	Blanking, Timing
			8	--
A	500A	740A	1	Call Light 0
			2	Call Light 1
			3	Call Light 2
			4	Call Light 3
			5	Call Light 4
			6	Call Light 5
			7	Call Light 6
			8	Call Light 7

Figure 2-7: 170E OUTPUT BOARD MEMORY MAP

2.6.6.4 **INPUT INTERFACE:** The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5VDC, shall be turned OFF (false) when the input current is less than 100 mA or the input voltage exceeds 8.5 VDC. Floating or unused inputs shall be pulled up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the CPU. Ground on any input shall be interpreted by the CPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the CPU when that input is read.

2.6.6.4.1 **INPUT BOARD MEMORY MAP** (READ):

INPUT PORT	170E ADDRESS	170E-ATC ADDRESS	BIT	FUNCTION
1	5001	7401	1	C1 – 39
			2	C1 – 40
			3	C1 – 41
			4	C1 – 42
			5	C1 – 43
			6	C1 – 44
			7	C1 – 45
			8	C1 – 46
2	5002	7402	1	C1 – 47
			2	C1 – 48
			3	C1 – 49
			4	C1 – 50
			5	C1 – 51
			6	C1 – 52
			7	C1 – 53
			8	C1 – 54
3	5003	7403	1	C1 – 55
			2	C1 – 56
			3	C1 – 57
			4	C1 – 58
			5	C1 –59
			6	C1 – 60
			7	C1 – 61
			8	C1 – 62
4	5004	7404	1	RESTART TIMER
			2	--
			3	--
			4	--
			5	C1 – 63
			6	C1 – 64
			7	C1 – 65
			8	C1 – 66
5	5005	7405	1	C1 – 67
			2	C1 – 68
			3	C1 – 69
			4	C1 – 70
			5	C1 – 71
			6	C1 – 72
			7	C1 – 73
			8	C1 – 74
6	5006	7406	1	C1 – 75
			2	C1 – 76
			3	C1 – 77
			4	C1 – 78
			5	C1 – 79
			6	C1 – 80
			7	C1 – 81
			8	C1 – 82
7	5007	7407	1	KEYPAD CONTACT

			2	KEYPAD CHAR LS
			3	KEYPAD CHAR NLS
			4	KEYPAD CHAR NMS
			5	KEYPAD CHAR MS
			6	STOP TIME SWITCH
			7	--
			8	--
8	5008	7408	1	--
			2	--
			3	--
			4	--
			5	--
			6	--
			7	--
			8	--

Figure 2-8: 170E INPUT BOARD MEMORY MAP

2.6.7 **MODEL 170E DATA AND ADDRESS BUS REQUIREMENTS**

2.6.7.1 All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 nsec.

2.6.7.2 All Address Bus Inputs shall be buffered, shall load the bus by 1 TTL gate load and 100 picofarads.

Section 7 CIRCUIT BOARDS

2.7.1 **GENERAL**

2.7.1.1 The Model 170E Controller Unit shall be modular in design. All Printed Circuit Boards (PCBAs) shall be vertically mounted.

2.7.1.2 All circuit boards shall be compatible with 170E Chassis and 170E-ATC Chassis.

2.7.1.3 All circuit boards shall be of double layer design.

2.7.1.4 All boards shall be uniquely keyed.

2.7.1.5 The motherboard shall have connectors with molded keys.

2.7.1.6 The Model 170E Controller Unit shall consist of the following:

Type 170E, 6802 Central Processing Unit (CPU) Board
Separate Input and Output Boards
Display Board (optional)
170E Chassis
Unit Power Supply with external power connection
Type 170E, Front Panel Assembly
Internal System Interface (Motherboard)
Connectors C1S, C2S, C20S, C30S, C40S, and T-1
Provisions for two Model 400 compatible DUAL MODEMS
A County approved 412 Series Memory Module
Provisions for a Caltrans Option Board

2.7.1.7 The composition weight shall not exceed 25 pounds (11.3 kg).

2.7.2 **CPU /MCU BOARDS, GENERAL**

2.7.2.1 NON-MASKABLE INTERRUPT, (NMI): The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the CPU NMI line to immediately go LOW. The line shall remain LOW until the RES goes LOW, to prevent multiple NMI issuances.

2.7.2.2 **RESET INTERRUPT (RES):** The RES is exclusively assigned to Power Restoration and CPU Startup. The RES line shall go LOW 3 ("1) msec following the NMI going LOW. The line shall remain LOW until 150 ("75) msec after Power Restoration.

2.7.2.3 **INTERRUPT REQUEST** (IRQ): The IRQ Line shall be jointly used by the RTC and ACIA's to initiate IRQ to the CPU.

2.7.2.4 **REAL TIME CLOCK (RTC):**. Real Time Clock Circuitry shall be provided to trigger an interrupt to the CPU on the IRQ line, and set bit 8 of the Status byte, **ONLY** once every 1/60 of a second, during the 270 degree to 330 degrees portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency.

2.7.2.5 **ACIA:** Four ACIA's, code compatible with the Motorola MC68B50, shall be provided. All ACIA's shall be capable of receiving and transmitting up to eight-bits of parallel data from the CPU for serial data communications. The ACIA's shall have 4 registers, which are addressable by the CPU. The CPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR), and writing to the Transmit Data Register (TDR) and the Control Register (CR).

2.7.2.6 **CPU/MPU CLOCK TIMING:** Clock circuitry shall be provided to generate the CPU clock timing.

2.7.2.6.1 The CPU clock circuitry shall be located within 2 inches (50.8MM) of the CPU clock input pins.

2.7.2.6.2 Selected CPU clock rate shall not affect the ACIA baud rates.

2.7.2.7 BAUD RATES: The following ACIA clock frequency / baud rate combinations shall be available:

CLOCK FREQ.	DIVIDE BY 16	DIVIDE BY 64

19.2 KHZ	1200 Baud	300 Baud
38.4 KHZ	2400 Baud	600 Baud
76.8 KHZ	4800 Baud	1200 Baud
153.6 KHZ	9600 Baud	2400 Baud
307.2 KHZ	19200 Baud	4800 Baud

Figure 2-9: ACIA CLOCK FREQ/BAUD RATES

2.7.2.8 Baud Rate shall be independently selectable for each ACIA by one of the means specified in Section 2.7.3.7 below.

2.7.2.9 **DOWNTIME ACCUMULATOR (DTA)**

2.7.2.9.1 A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon Power Failure and continue counting until the RES line goes HIGH following Power Restoration.

2.7.2.9.2 The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be "250 msec over the 255-minute range. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and the Seconds Register reset to "0". When the Minutes reach 255, the DTA MAXOUT bit (bit 7) of the Status Byte shall be set, and the DTA shall stop counting.

2.7.2.9.3 Once the Minutes Register reaches maximum count, it shall remain latched in this condition until reset by software following Power Restoration.

2.7.2.9.4 All DTA circuitry, including the Unit Standby Power source, shall be located on one board.

2.7.2.10 **RESTART TIMER**: A Restart Timer Circuit shall be provided to react to the duration of power outage. The Restart Timer output state is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 ("0.25) seconds, its output state shall go to LOW and remain in that state for 50 ("24) msec after the RES line goes HIGH. If power is restored prior to the timer, timing out, the output shall remain HIGH and the timer shall be reset to "0".

2.7.2.11 **MODEM AND ACIA REQUIREMENTS**

2.7.2.11.1 The interface between the ACIA's and the MODEMS shall comply with EIA RS-232-C Standards. The RTS and TX DATA lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12 VDC respectively.

2.7.2.11.2 A Modem connector and interface, compatible with the Model 400 Dual Modem, and CPU ACIA, designated ACIA #1 and #2, shall be provided. Connections into and out of the controller unit shall be made through Connector C2S, C20S. The control and data transmission lines from Connector C2S shall be paralleled through Terminal Block T-1 (TYPE T Connector).

2.7.2.11.3 A second Modem connector and interface, compatible with the Model 400 Dual Modem, and two ACIA's, designated as ACIA #3 and #4, shall be provided, with access via connector C30S and C40S.

2.7.2.11.4 The C2S, C20S, C30S, and C40S connectors shall all be mounted on the rear panel of the controller.

2.7.3 **TYPE 6802 CPU BOARD:**

2.7.3.1 The 6802 CPU board shall have provisions for on-board RAM and EPROM. The LS socket shall be fully decoded for a 32KByte NOV-RAM, and the MS socket shall accommodate a 32KByte EPROM. Jumpers on the CPU board shall be used to select internal memory (CPU) and/or external memory (Memory Module). (see memory map)

2.7.3.2 The CPU Board shall be provided with an CPU and shall properly execute object programs developed to operate on the 6800/6802 CPU. The CPU interrupt requirements are defined in section 2.7.2 above “CENTRAL PROCESSING UNIT (CPU) BOARD GENERAL”.

2.7.3.3 Means shall be provided to independently disconnect the IRQ from each ACIA.

2.7.3.4 The capability to exchange the addresses of ACIA #2 and ACIA #3 shall be accomplishes by shunt jumper(s).

2.7.3.5 Two selectable CPU machine cycle times shall be provided: 1.302 and 0.651 ("0.0015) Fsec, corresponding to clock rates of 3.072 MHz and 6.144 MHz.

2.7.3.6 Selected CPU clock rate shall not affect the ACIA baud rates.

2.7.3.7 To facilitate selection of CPU speed, CPU board/Memory Module memory option, baud rates, and ACIA IRQ disconnect, as stipulated in this specification, pads spaced at 0.1" centers shall be provided on the circuit board. Connection between the pads for desired settings shall be accomplished by one of the following methods: (Option A or B to be determined at the time of ordering)

Option A: Soldered jumper wire
Option B: Wire-wrap posts with removable shunt jumpers

2.7.4 **The INPUT BOARD** shall contain only the 170E - 170E-ATC controller input circuitry (and the DTA if it is not on the CPU board).

2.7.5 **The OUTPUT BOARD** shall contain only the 170E - 170E-ATC controller output circuitry.

2.7.6 **The OPTIONAL DISPLAY BOARD** shall contain only the circuitry needed to run the front panel display and keyboard.

Section 8 MODEL 412F MEMORY MODULE:

2.8.1.1 **MEMORY MODULE DESCRIPTION**: the 412F Memory Module shall be designed to work with all Model 170 controllers and Model 170E Controllers. It is not used in the Model 170E-ATC Controller. CPU board configuration jumpers allow all of the program memory and a 4 K byte sub-block of RAM memory to be internal or external to the CPU board. The four Kbyte sub-block of RAM resides at different address between the two different processors ($7000 with the 6802 CPU and $6000 with the 68HC11 MCU). The 412F Memory Module uses a PCBA mounted address switch making the memory module compatible with both types of CPU and MCU PCBAs.

2.8.1.2 The 412F shall also bring communication port C40 to the front panel. All control lines shall be user configurable to adapt to any configuration (three wire or hardwire flow control).

2.8.1.3 The memory module shall be designed to eliminate the need for a battery and associated circuitry, through the exclusive use of non-volatile RAM devices (NOV-RAM).

2.8.1.4 ACIA serial port #4 will be paralleled over to the Memory Module and option board connectors along with NMI, RES and ROT.

2.8.2 **MODEL 412F MODULE REQUIREMENTS:**

2.8.2.1 The Memory Module slot shall accept all Memory Modules designed for any Model 170 Controller. The +5VDC requirements of the Memory Module shall be derived only from the +12VDC controller power supply.

2.8.2.2 The Memory Module board dimensions, contact assignments, and space requirements shall comply with the details shown on the plans.

2.8.2.3 Any Memory Module incorporating variations or additions to this specification must be submitted to the County for approval prior to delivery of a Sample Unit.

2.8.2.4 Unless otherwise specified, one Memory Module shall be delivered with each 170E controller. One EPROM device shall be included, mounted in the EPROM socket. One NOV-RAM memory device shall be included, mounted in the NRAM socket.

2.8.2.5 All PCBA connectors shall be provided with electrostatic charge protection to prevent CMOS device damage.

2.8.2.6 The Memory Module's front panel shall be connected to Equipment Ground at M/170 Pin 34.

2.8.2.7 All addressable devices shall be fully decoded.

2.8.2.8 Sockets for EPROM and NRAM chips shall be marked on the board adjacent to each socket designating the following descriptors, EPROM and NRAM.

2.8.2.9 All electrical connections in and out of this module (excluding Port C40) shall be through a printed circuit connector having two rows of 36 independent bifurcated contacts on 0.100-inch centers.

2.8.2.10 **DOCUMENTATION**: The Vendor shall furnish one manual for each memory module delivered. The Manual shall include, but not be limited to:

1. Theory of Operation
2. Device Table to correlate selected Memory Addressing with the Decode Program options and related Jumper Selections.
3. Complete Program listing covering all the Program Options that could be resident in the Decode PROM's.
4. Complete Schematics
5. Assembly drawings with Component layout
6. Parts List reflecting Circuit Symbols and Manufacturer's Part Number.
7. Data Sheets covering medium and large scale Integrated Circuits.

2.8.2.11 **FUNCTIONAL REQUIREMENTS**

2.8.2.11.1 All data inputs and outputs shall be tri-state buffered on this module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed, the data

output shall be disabled into a high impedance state and the data I/O lines shall not source or sink more than 100 microamperes.

2.8.2.11.2 All address inputs shall not load the bus by more than one TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 nanoseconds.

2.8.2.11.3 Circuitry shall be provided on the module to protect memory device data from damage in the event of AC power outages or fluctuations.

2.8.2.12 POWER REQUIREMENTS

2.8.2.12.1 The Memory Module shall incorporate an on-board +5 VDC three terminal regulator sourced from the controller +12 VDC supply. The regulator shall have a minimum efficiency of 75%, and shall supply +5 (±0.1) VDC from no load to a maximum load of 450 mA with no more than 2% ripple.

2.8.2.13 ACIA serial port #4 will be paralleled over to the Memory Module and option board connectors along with NMI, RES and ROT.

2.8.2.14 MEMORY REQUIREMENTS:

2.8.2.14.1 The Memory Module shall provide a minimum of 64K 8-bit words of EPROM memory in two software banks of 32K bytes each. Each EPROM chip shall be electrically programmable and shall be erasable by exposure to ultraviolet radiation. This memory shall be non-volatile and shall not be affected by transients resulting from power switching and external loading and unloading conditions. Two clearly labeled sockets shall be provided to accommodate memory devices.

2.8.2.14.2 The EPROM chip shall be jumper selectable as a 32K X 8 (INTEL 27C256), 64K x 8 (INTEL 27C512), or a 128K x 8 INTEL 27C010) device.

2.8.2.14.3 The supplied EPROM chip shall be a 128K x 8 device or equivalent.

2.8.2.14.4 The NRAM MEMORY devices supplied for the Memory Module shall be 32KByte DALLAS 1230Y, or equivalent.

2.8.2.14.5 MODEL 412F MEMORY MAP ADDRESS RANGES

EPROM	**BANK**
$18000 - $1FFFF	HIGH
$08000 - $0FFFF	LOW
RAM	PCBA SWITCH
$1000 - $6FFF	68HC11
$1000 - $4FFF and $7000 - $7FFF	6800
BLANK SELECTION	
$FFF0 (On Write)	Sets Bank line Low
$FFF1 (On Write)	Sets Bank line High
$FFFE (Read or Write)	Sets Bank line High

Figure 2-10: MODEL 412F MEMORY MAP

2.8.2.14.6 MODEL 412F MODULE MEMORY MAP SELECTOR SWITCH

2.8.2.14.7 The PCBA mounted address switch selects one of two address decodes to enable the 4 K byte block of NRAM to be swapped. Selecting either map placed the data in the same 4 K byte block of NRAM on the 412F. This allows the user to save timing from a 170E running a 6802 CPU and down load to a 170E - 170E-ATC controller running a 68HC11 MCU.

PCBA SWITCH POS.	NRAM ADDRESS RANGE (4K block)
6800	$7000 - $7FFF
68HC11	$6000 - $6FFF

Figure 2-11: 412F ADDRESS SWITCH

2.8.2.14.8 MODEL 412F COMMUNICATIONS PORT C40 JUMPER POSTS

A1 (to DB9-1)	B1 (to DCD)	C1 (to +12vdc)
A2 (to C3 & TXD)	B2 (to DB9-2)	C2 (to A3 & RXD)
A3 (to C2 & RXD)	B3 (to DB9-3)	C3 (to A2 & TXD)
A4 (to C5 & CTS)	B4 (to DB9-7)	C4 (to A5 & RTS)
A5 (to C4 & RTS)	B5 (to DB9-8)	C5 (to A4 & CTS)
Note: DB9-5 is DC COMMON. For hardware flow control, jumper A1 to B1, and A5 to B5. For three wire operation, jumper B1 to C1, B3 to C3, and C4 to C5.		

Figure 2-12: 412F COMM PORT JUMPERS

2.8.2.15 **CALTRANS OPTION BOARD:**

2.8.2.15.1 **DESCRIPTION:** The Caltrans Option Board slot shall accept all Caltrans Option boards. The Option board connector will be referred to as "M/170E". This connector will be the same as the M/170 (Memory Module) connector with the same pin assignments. The connecting PCBA will be the same size as the Model 400 Modem. The PCBA edge connector pin assignments and spacing will match and mate with the M/170E.

2.8.2.15.2 The Caltrans Option Board will house the internal RTCA and I.D switches

2.8.2.15.3 The M/170 connector, pin 72 will be separated from the GND function and be routed to pin 72 of the M/170E connector. The purpose of this sense line is to override the Option board if the operator inadvertently plugs in an external Memory Module.

2.8.2.15.4 ACIA serial port #4 will be paralleled over to the Memory Module and option board connectors along with NMI, RES and ROT.

2.8.2.15.5 **GENERAL REQUIREMENTS**

2.8.2.15.5.1 All module's PCBA Connectors shall be provided with electrostatic charge protection to prevent CMOS device damage.

2.8.2.15.5.2 All addressable devices shall be fully decoded.

2.8.2.15.5.3 All electrical connections in and out of this module shall be through a printed circuit connector having two rows of 36 independent bifurcated contacts on 0.100-inch centers.

2.8.2.15.6 **DOCUMENTATION**

2.8.2.15.6.1 The Vendor shall furnish one manual for each module delivered. The Manual shall include, but not be limited to:

1. Theory of Operation
2. Device Table to correlate selected Memory Addressing with the Decode Program options and related Jumper Selections.
3. Complete Program listing covering all the Program Options that could be resident in the Decode PROM's.
4. Complete Schematics
5. Assembly drawings with Component layout
6. Parts List reflecting Circuit Symbols and Manufacturer's Part Number.
7. Data Sheets covering medium and large scale Integrated Circuits.

2.8.2.15.7 **FUNCTIONAL REQUIREMENTS**

2.8.2.15.7.1 All data inputs and outputs shall be tri-state buffered on this module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed, the data output shall be disabled into a high impedance state and the data I/O lines shall not source or sink more than 100 microamperes.

2.8.2.15.7.2 All address inputs shall not load the bus by more than 1 TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 nanoseconds.

2.8.2.15.7.3 Circuitry shall be provided on the module to protect memory device data from damage in the event of AC power outages or fluctuations.

2.8.2.16 **POWER REQUIREMENTS**

2.8.2.16.1 The module shall incorporate an on-board +5 VDC three terminal regulator sourced from the controller +12 VDC supply. The regulator shall have a minimum efficiency of 75%, and shall supply +5 (±0.1) VDC from no load to a maximum load of 450 mA with no more than 2% ripple.

Section 9 FRONT PANEL

2.9.1 The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous stainless steel or aluminum piano hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

2.9.2 An approved latch mechanism shall be provided to secure the right side of the front panel to the chassis.

2.9.3 The front panel shall be electrically connected by means of Connector C3.

2.9.4 The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 0.40-inch high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the CPU through the output interface to the display shall result in the display of each character in its non-inverted state.

2.9.5 The front panel shall be provided with 10 LED indicators, labeled "CALL/ACTIVE" and numbered "0" through "9" to the right or left of each indicator.

2.9.6 The front panel MAY include an LED indicator displaying the "Watchdog" output, labeled same or "WDT". The "Battery Charging" LED indicator no longer required may be used for this purpose.

2.9.7 A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the CPU shall result in each character being received in its non-inverted state. The character shall consist of four bits of binary data, while the character control shall consist of one bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 0.075 square inch and shall be mounted on a minimum of 0.50-inch center; shall have an actuation threshold between 50 and 100 grams and shall provide a positive tactical indication of contact. Key contacts shall have design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 msec following contact opening.

2.9.8 The front panel shall be provided with a toggle switch to enable the stop timing function and shall be labeled "STOP TIMING".

2.9.9 An AC POWER toggle switch and fuse shall be provided. The switch and fuse shall protrude through the front panel, but not be attached (they shall remain with the modular Power Supply when the front panel is opened or removed). The fuse shall be a 3AG Type rated at 150% of unit load.

Section 10 DIAGNOSTIC AIDS

2.10.1 Extender Boards, wrap-around cables, and test jigs shall be available from the manufacturer, at the time of equipment purchase, and in quantities determined at the time of purchase.

2.10.2 The Contractor shall furnish a Diagnostic Test Program, resident in the provided EPROM, in each controller unit, at the time of delivery. The Program shall test and report failures on all functions and circuits within the 170E controller. This Program shall meet the following requirements.

2.10.3 Five copies of a 170E Diagnostic Test Program Software Manual shall be supplied. The Manual shall include full and complete documentation of test procedures, including, but not limited to the following:

170E Verification Test Operation
Individual Diagnostic Tests
Program listings in assembly format, with detailed comments
Detailed flow charts, which are keyed to the software listing using instruction labels and subroutine names.

2.10.4 The Diagnostic Test Program shall be an integrated Front Panel and CRT/Keyboard program.

2.10.5 The Diagnostic Test Program shall include, but not be limited to, the following capabilities:

Display Test Results
Display Number of Test Performed
Display Accumulated Number of Test Failed
Display Start Up Test Results
Automatic Cyclic Test
Manual Test Selection and Repeat of a Single Test (loop)
ACIA #1 with and without Modem
ACIA #2 with and without Modem
ACIA #3 with and without Modem
ACIA #4 with and without Modem

2.10.5.1 **START-UP TESTS**:

RAM Identify - size and address
RAM Pretest
RAM Retention
Number of NMI's
Number of Resets
Restart Timer
DTA Display

2.10.5.2 **AUTOMATIC TESTS:**

RAM Short
RAM Extensive
Memory Module RAM
I/O Wrap-Around
Real Time Clock
Display
Keyboard
ACIA #1 with Modem
ACIA #1 without Modem
ACIA #2 with Modem
ACIA #2 without Modem
ACIA #3 with Modem
ACIA #3 without Modem
ACIA #4 with Modem
ACIA #4 without Modem
CPU Instruction
System Addressing
EPROM Checksum

2.10.6 The Diagnostic Program, when performing the Input/Output wrap-around test, shall incorporate the Input Port/Output Port addressing as specified in Figure 1-1.

2.10.7 The C1 wrap-around connector shall be wired as shown below.

C1 WRAP-AROUND CONNECTOR PIN-OUT											
JUMPER						JUMPER					
FROM C1 OUTPUT			TO C1 INPUT			FROM C1 OUTPUT			TO C1 INPUT		
PIN	PORT	BIT	PIN	PORT	BIT	PIN	PORT	BIT	PIN	PORT	BIT
2	01	1	39	01	1	35	05	1	67	05	1
3	01	2	40	01	2	36	05	2	68	05	2
4	01	3	41	01	3	37	05	3	69	05	3
5	01	4	42	01	4	38	05	4	70	05	4
6	01	5	43	01	5	100	05	5	71	05	5
7	01	6	44	01	6	101	05	6	72	05	6
8	01	7	45	01	7	102	05	7	73	05	7
9	01	8	46	01	8	103	05	8	74	05	8
10	02	1	47	02	1	83	06	1	75	06	1
11	02	2	48	02	2	84	06	2	76	06	2
12	02	3	49	02	3	85	06	3	77	06	3
13	02	4	50	02	4	86	06	4	78	06	4
15	02	5	51	02	5	87	06	5	79	06	5
16	02	6	52	02	6	88	06	6	80	06	6
17	02	7	53	02	7	89	06	7	81	06	7
18	02	8	54	02	8	90	06	8	82	06	8
19	03	1	55	03	1	91	07	1	75	06	1
20	03	2	56	03	2	93	07	2	76	06	2
21	03	3	57	03	3	94	07	3	77	06	3
22	03	4	58	03	4	95	07	4	78	06	4
23	03	5	59	03	5	96	07	5	79	06	5

24	03	6	60	03	6	97	07	6	80	06	6
25	03	7	61	03	7	98	07	7	81	06	7
26	03	8	62	03	8	99	07	8	82	06	8
27	04	1	55	03	1						
28	04	2	56	03	2						
29	04	2	57	03	3						
30	04	4	58	03	4						
31	04	5	59	03	5	1	LOGIC GND		63	04	5
32	04	6	60	03	6	14	LOGIC GND		64	04	6
33	04	7	61	03	7	92	LOGIC GND		65	04	7
34	04	8	62	03	8	104	LOGIC GND		66	04	8

Figure 2-13: C1 WRAP-AROUND CONNECTOR PIN-OUT

2.10.8 The C2, C20, C30, and C40 wrap-around connectors (with Modem) shall be wired as shown below.

C2, C20, C30, C40 WRAP-AROUND (MODEM) CABLE WIRE LIST			
From Pin	**Function**	**To Pin**	**Function**
A	Audio In	C	Audio Out
B	Audio In	E	Audio Out
NOTE: Audio In / Audio Out - refers to In/Out of a MODEM			

Figure 2-14: C2, C20, C30, C40 Warp-Around (Modem) Cable Wire List

2.10.9 The C2, C20, C30, and C40 wrap-around connectors (without Modem) shall be wired as shown below.

C2, C20, C30, C40 WRAP-AROUND (ACIA) CABLE WIRE LIST			
From Pin	**Function**	**To Pin**	**Function**
J	RTS	M	CTS
J	RTS	H	DCD
K	DATA IN	L	DATA OUT
NOTE: Data In / Data Out - refers to In/Out of a MODEM			

Figure 2-15: C2, C20, C30, C40 Warp-Around (ACIA) Cable Wire List

Section 11 MODEL 400 MODEM MODULE

2.11.1 The MODEM shall provide two-wire half-duplex and four-wire full duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN/OUT.

2.11.2 The MODEM shall be compatible with Bell Standard 202S and comply with the following requirements:

2.11.2.1 **DATA RATE**: 300 to 1200 baud modulation.

2.11.2.2 **MODULATION**: Phase coherent frequency shift keying (FSK).

2.11.2.3 **DATA FORMAT**: Asynchronous, serial by bit.

2.11.2.4 **LINE AND SIGNAL REQUIREMENTS**: Type 3002 voice-grade, unconditioned.

2.11.2.5 **ACIA and MODEM INTERFACE**: EIA RS-232-C standards.

2.11.2.6 **TONE CARRIER FREQUENCIES** (Transmit & Receive): 1200 Hz (MARK) and 2200 Hz (SPACE) with ±1% tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

2.11.2.7 **TRANSMITTING OUTPUT SIGNAL LEVEL**: 0, -2, -4, -6, and -8 dBm (at 1700 Hz) continuous or switch selectable.

2.11.2.8 **RECEIVER INPUT SENSITIVITY**: 0 to -40 dBm.

2.11.2.9 **RECEIVER BAND PASS FILTER**: Shall meet the error rate requirement specified in Paragraph 2.10.2.15 and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

2.11.2.10 **CLEAR-TO-SEND (CTS)** DELAY: 12 (±2) msec.

2.11.2.11 **RECEIVE LINE SIGNAL DETECT TIME**: 8 (±2) msec mark frequency.

2.11.2.12 **RECEIVE LINE SQUELCH**: 6.5 (±1) msec, 0 msec (OUT).

2.11.2.13 **SOFT CARRIER (900 Hz) TURN OFF TIME**: 10 (±2) msec.

2.11.2.14 **MODEM RECOVERY TIMER**: Capable of receiving data within 22 msec after completion of transmission.

2.11.2.15 **ERROR RATE:** Shall not exceed 1 bit in 100,000 bits, with a signal- to-noise ratio of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

2.11.2.16 **TRANSMIT NOISE**: Less than 50 dB across 600 ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

2.11.2.17 The MODEM power requirements are as follows:

Input Voltages	Maximum Current Consumption
+12 VDC	75 mA
-12 VDC	75 mA

2.11.3 Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data

2.11.4 MODEL 400 DUAL MODEM PIN-OUT

MODEL 400 DUAL MODEM PIN-OUT			
Pin	**Function**	**Pin**	**Function**
2	Modem 1 AUDIO IN	A	DC GROUND
3	Modem 1 AUDIO IN	B	DC GROUND
9	ACIA 2 DCD	C	+12 VDC
10	ACIA 2 RTS	D	+12 VDC
11	ACIA 2 DATA IN	E	-12 VDC
12	ACIA 2 CTS	F	-12 VDC
13	ACIA 2 DATA OUT	K	ACIA 1 DCD
19	Modem 2 AUDIO OUT	L	ACIA 1 RTS
20	Modem 2 AUDIO OUT	M	ACIA 1 DATA IN
21	Modem 2 AUDIO IN	N	ACIA 1 CTS
22	Modem 2 AUDIO IN	P	ACIA 1 DATA OUT
		X	Modem 1 AUDIO OUT
		Y	Modem 1 AUDIO OUT

Figure 2-16: Model 400 Dual Modem Pin-out

Section 12 CHAPTER DETAILS

2.12.1 MODEL 170E CONTROLLER UNIT DIAGRAM

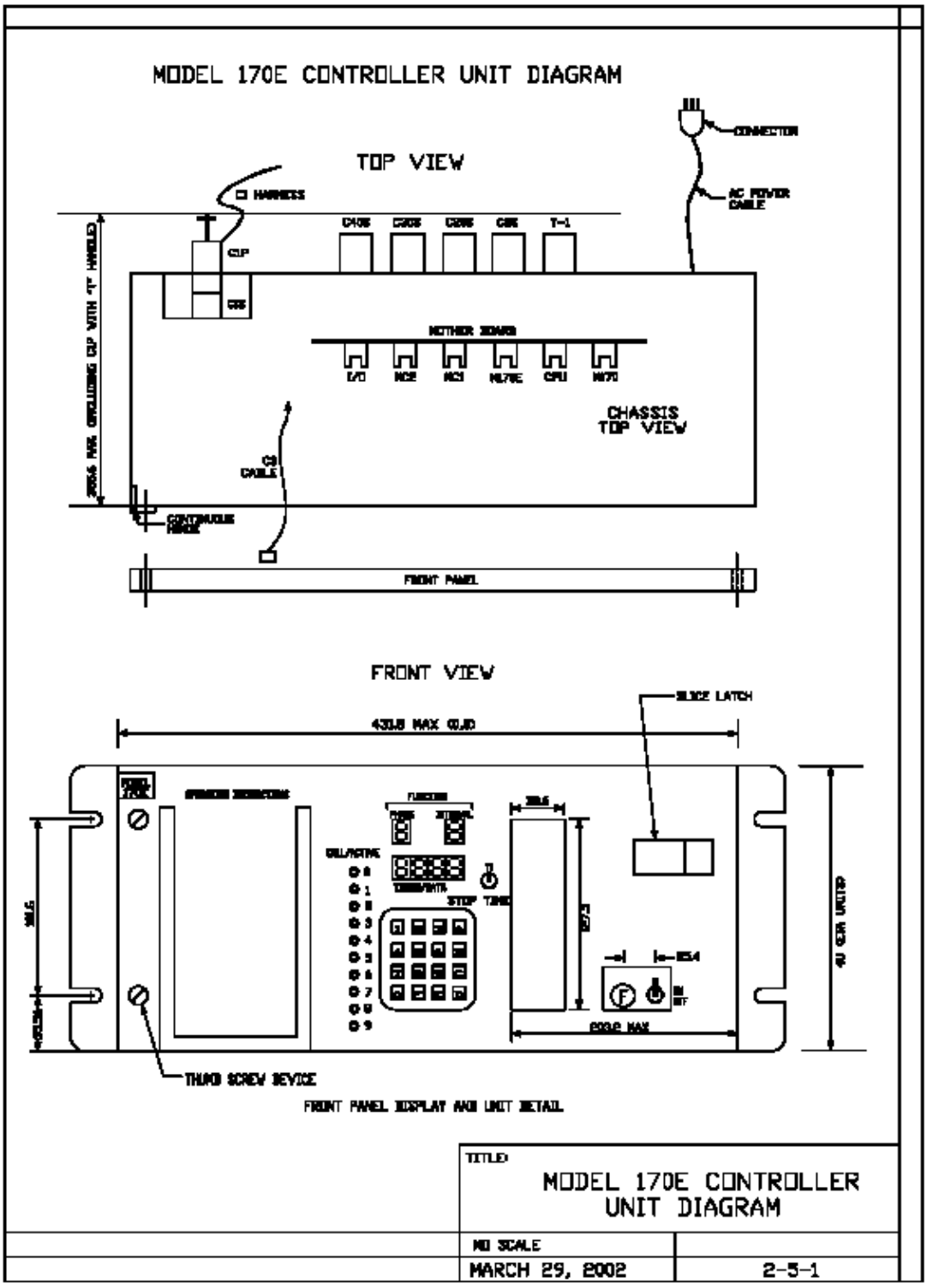


Figure 2-17: TEES DRAWING 2-5-1, MODEL 170E CONTROLLER UNIT DIAGRAM

2.12.2 MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

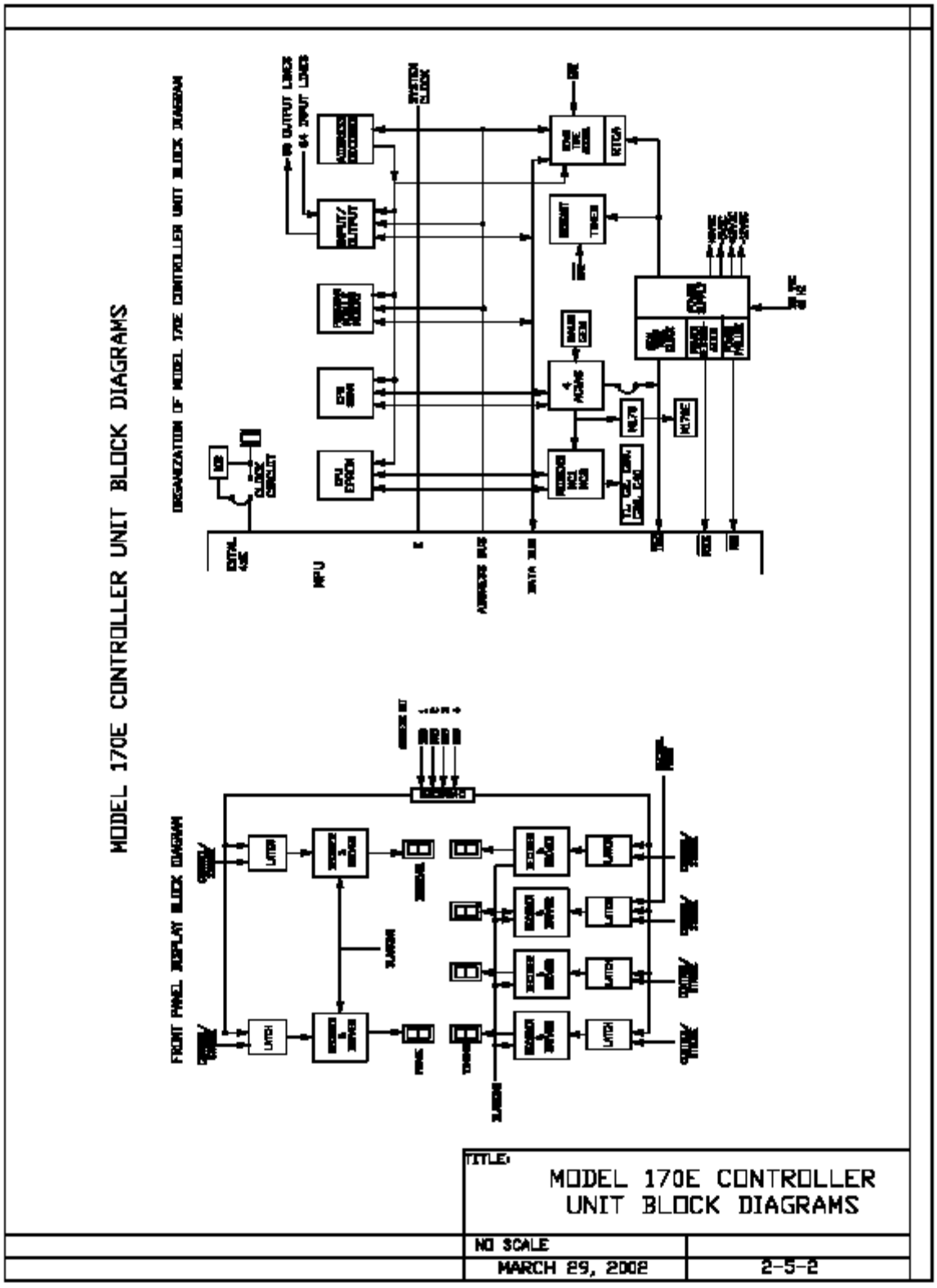


Figure 2-18: TEES DRAWING 2-5-2, MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

2.12.3 INPUT PORT ADDRESS ASSIGNMENTS

INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	
5001	1	39	5005	1	67	
5001	2	40	5005	2	68	
5001	3	41	5005	3	69	
5001	4	42	5005	4	70	
5001	5	43	5005	5	71	
5001	6	44	5005	6	72	
5001	7	45	5005	7	73	
5001	8	46	5005	8	74	
5002	1	47	5006	1	75	
5002	2	48	5006	2	76	
5002	3	49	5006	3	77	
5002	4	50	5006	4	78	
5002	5	51	5006	5	79	
5002	6	52	5006	6	80	
5002	7	53	5006	7	81	
5002	8	54	5006	8	82	
5003	1	55	5007	1		KEYBOARD CONTROL
5003	2	56	5007	2		KEYBOARD CH LS
5003	3	57	5007	3		KEYBOARD CH NLS
5003	4	58	5007	4		KEYBOARD CH NMS
5003	5	59	5007	5		KEYBOARD CH MS
5003	6	60	5007	6		STOP TIMING
5003	7	61	5007	7		NA
5003	8	62	5007	8		NA
5004	1	NA	5008	1		NA
5004	2	NA	5008	2		NA
5004	3	NA	5008	3		NA
5004	4	NA	5008	4		NA
5004	5	63	5008	5		NA
5004	6	64	5008	6		NA
5004	7	65	5008	7		NA
5004	8	66	5008	8		NA

CONNECTOR C2 SOCKET ASSIGNMENT (C20, C30 & C40)

C2 SOCKET CONTACTS	C2 FUNCTION	C2 SOCKET CONTACTS	C2 FUNCTION
A	Audio IN	J	RTS
B	Audio IN	K	Data IN
C	Audio OUT	L	Data OUT
D	+5VDC	M	CTS
E	Audio OUT	N	DC GND
F	-5VDC	P	NA
H	CD	R	NA

TERMINAL BLOCK T-1 ASSIGNMENTS

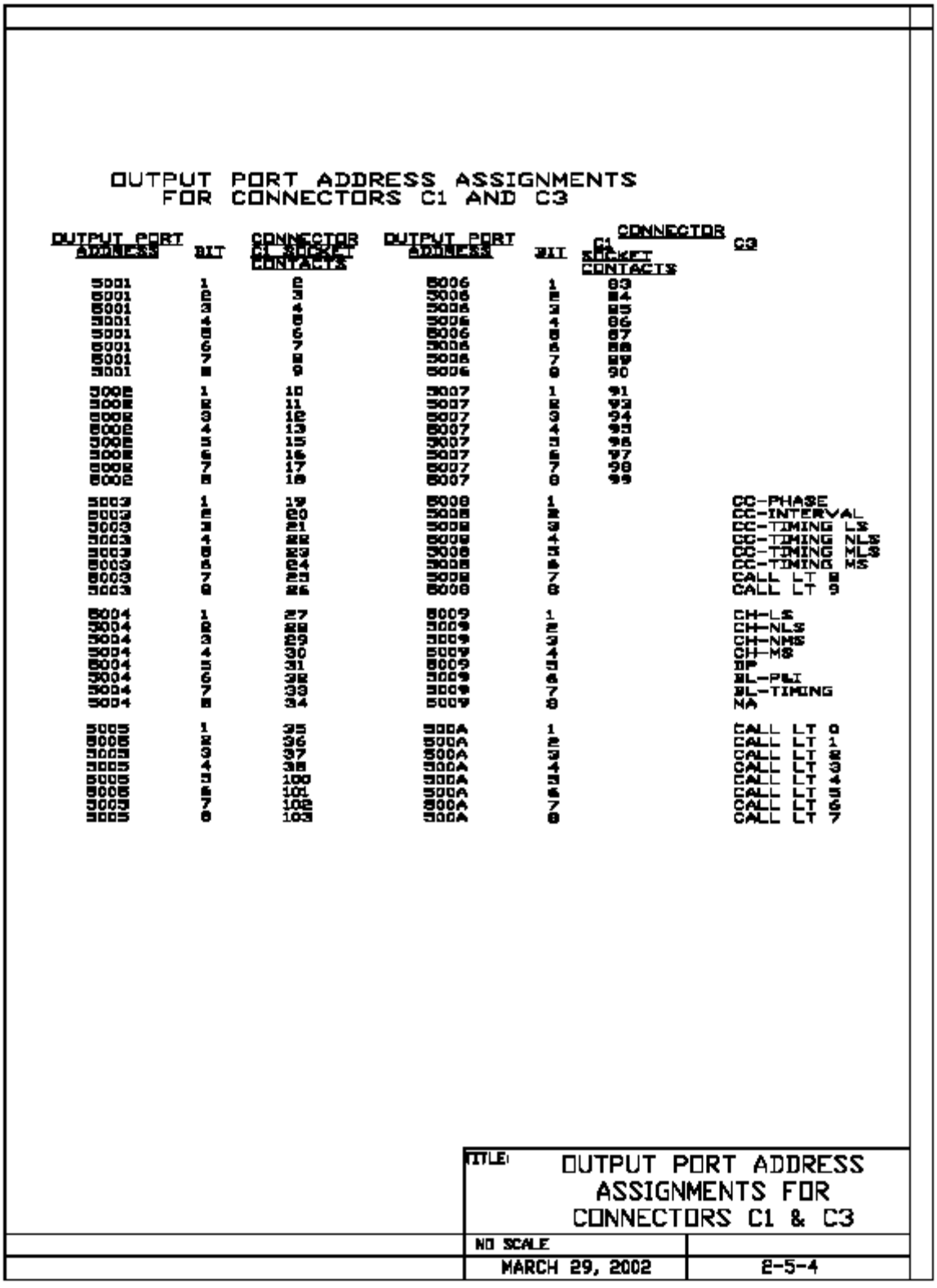
1. Audio IN
2. Audio IN
3. CD
4. RTS
5. Data IN
6. CTS
7. Data Out
8. Audio Out
9. Audio Out
10. DC GND

TITLE:
MODEL 170E INPUT ADDRESS

NO SCALE
MARCH 29, 2002
2-5-3

Figure 2-19: TEES DRAWING 2-5-3, INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3 (6802 MPU MODULE)

2.12.4 OUTPUT PORT ADDRESS ASSIGNMENTS



OUTPUT PORT ADDRESS ASSIGNMENTS
FOR CONNECTORS C1 AND C3

OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	OUTPUT PORT ADDRESS	BIT	CONNECTOR C3 SOCKET CONTACTS	
5001	1	2	5006	1	83	
5001	2	3	5006	2	84	
5001	3	4	5006	3	85	
5001	4	5	5006	4	86	
5001	5	6	5006	5	87	
5001	6	7	5006	6	88	
5001	7	8	5006	7	89	
5001	8	9	5006	8	90	
5002	1	10	5007	1	91	
5002	2	11	5007	2	92	
5002	3	12	5007	3	94	
5002	4	13	5007	4	95	
5002	5	15	5007	5	96	
5002	6	16	5007	6	97	
5002	7	17	5007	7	98	
5002	8	18	5007	8	99	
5003	1	19	5008	1		CC-PHASE
5003	2	20	5008	2		CC-INTERVAL
5003	3	21	5008	3		CC-TIMING LS
5003	4	22	5008	4		CC-TIMING NLS
5003	5	23	5008	5		CC-TIMING MLS
5003	6	24	5008	6		CC-TIMING MS
5003	7	25	5008	7		CALL LT 8
5003	8	26	5008	8		CALL LT 9
5004	1	27	5009	1		CH-LS
5004	2	28	5009	2		CH-NLS
5004	3	29	5009	3		CH-NMS
5004	4	30	5009	4		CH-MS
5004	5	31	5009	5		BP
5004	6	32	5009	6		BL-PLI
5004	7	33	5009	7		BL-TIMING
5004	8	34	5009	8		NA
5005	1	35	500A	1		CALL LT 0
5005	2	36	500A	2		CALL LT 1
5005	3	37	500A	3		CALL LT 2
5005	4	38	500A	4		CALL LT 3
5005	5	100	500A	5		CALL LT 4
5005	6	101	500A	6		CALL LT 5
5005	7	102	500A	7		CALL LT 6
5005	8	103	500A	8		CALL LT 7

	TITLE: OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 & C3	
	NO SCALE	
	MARCH 29, 2002	2-5-4

Figure 2-20: TEES DRAWING 2-5-4, OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3 (6802 MPU MODULE)

2.12.5 MODEL 400 MODEM MODULE

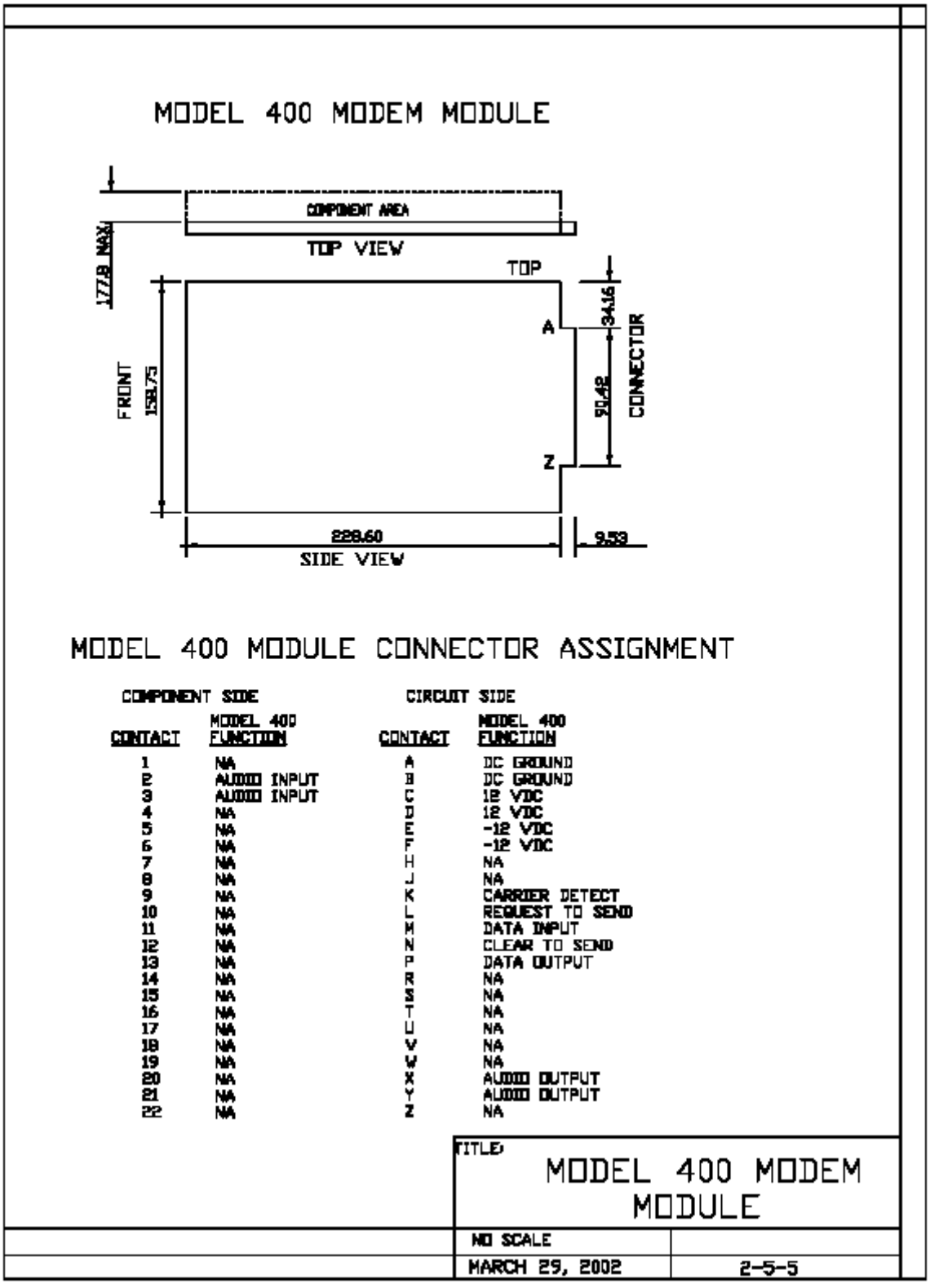


Figure 2-21: TEES DRAWING 2-5-5, MODEL 400 MODEM MODULE

2.12.6 TYPE 412 SYSTEM MEMORY MODULE

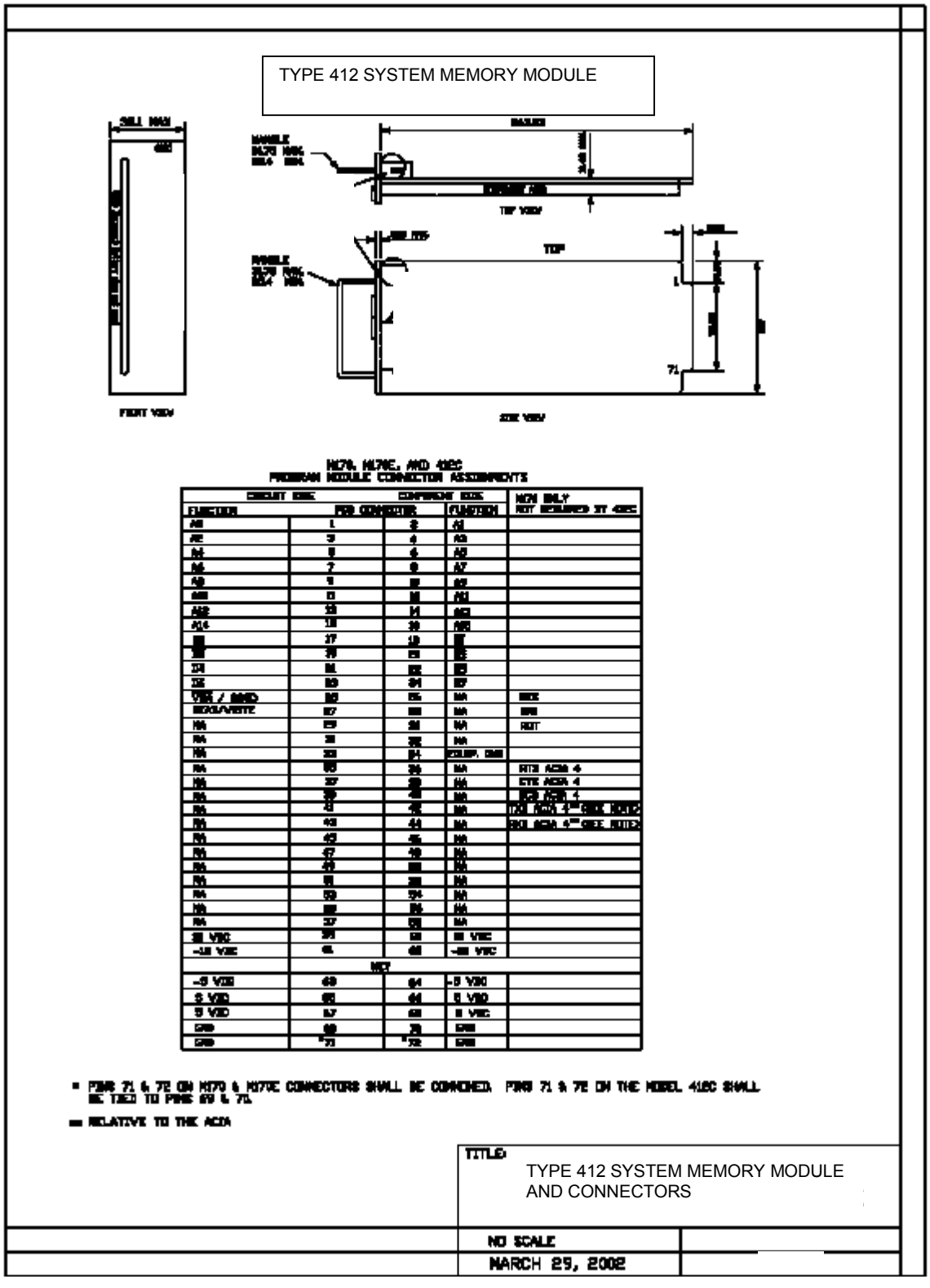


Figure 2-22: TEES DRAWING 2-5-6, TYPE 412 SYSTEM MEMORY MODULE

CHAPTER 3 MODEL 170E-ATC CONTROLLER

Section 1 GENERAL

3.1.1 **DESCRIPTION:** the 170E-ATC Controller is an upgrade of the 170E Controller. It uses a **MC68HC11F1 (HC11)** type MCU Board installed in a 170E-ATC Chassis. The 170E-ATC Controller retains the 170E type front panel, but not the type 412 Memory Module. All NRAM and EPROM are on the MCU Board. The NRAM is a **DS1744** Nonvolatile RAM with an integrated real-time clock. The memory map setup is software configurable. Communication is thru a **ST16C654** QUAD UART with four type 400 modem slots. The controller is upgradeable to emulate a 2070L ATC Controller. The ATC-HC11 MCU Board also has a Communication port to drive a type 2070 front panel.

3.1.2 **POWER FAILURE**: A power failure is said to have occurred when the incoming line voltage falls below 92 ±2) VAC for 50 msec. The determination of the 50 msec interval shall be completed within 67 msec of the time the voltage falls below 92 (±2) VAC.

3.1.3 **POWER RESTORATION**: Power is considered restored when the incoming line voltage equals or exceeds 97 (±2) VAC for 50 msec. The determination of the 50 msec interval shall be completed within 67 msec of the time the voltage first reaches 97 (±2) VAC.

3.1.4 **POWER HYSTERESIS:** The hysteresis between power failure and power restoration voltage settings shall be a minimum of 5 volts and a maximum of 6 volts.

3.1.5 Each memory device shall stabilize to normal operation within 10 msec following Power Restoration and shall be in Standby until addressed.

3.1.6 All memory devices shall be second sourced and shall operate over the specified electrical and environmental ranges of the controller unit, and shall have access times at or below 200 nanoseconds see 3.1.10 below.

3.1.7 Spare Modules: The manufacturer shall provide one complete set of replacement modules for every 100 controller-units purchased on a contract. One set of complete replacement modules is listed as following:

1. 170E ATC-HC11 MCU Board
2. 170E Input Board
3. 170E Output Board
4. 170E Display Board (if used)
5. 170E Front Panel Board and Keypad (s)
6. Unit Power Supply
7. Any other circuit boards used.

3.1.8 **EPROM MEMORY:**

3.1.8.1 The EPROM supplied with the 170E-ATC shall be 128K x8 (ceramic INTEL 27C010), equivalent hereafter referred to as "EPROM."

3.1.9 **Nonvolatile RAM MEMORY:** All RAM supplied shall be Non-Volatile as described below, hereafter referred to as "**NOV-RAM**" or "**NRAM**".

3.1.9.1 Each NOV-RAM device shall be mounted in a Memory Assembly. The Memory Assembly shall incorporate a self-contained Lithium energy source with control circuitry that automatically protects data during loss of power. RAM data retention shall be a minimum of 10 years from date of assembly manufacture.

3.1.9.2 The supplied device shall be a DALLAS DS1744, 32K byte NRAM with built in Real Time Clock, or equivalent.

3.1.9.3 Optionally a DALLAS 1230Y, NOV-RAM MEMORY or equivalent may be specified at the time of order.

3.1.9.4 Only Memory Assemblies manufactured within the previous 12 months shall be delivered to the County. The month and year of manufacture shall be clearly and permanently marked on the top of the device.

3.1.10 The total READ/WRITE time including buffering, decoding, device access time and accessed data presented to the controller unit data bus shall not exceed 200 **0**sec. Memory devices shall have read and write time suitable to perform either function in one MCU instruction cycle.

3.1.11 Socket mounting shall be permitted **ONLY** for MCU, NRAM, UART, EPROM devices and Programmable devices if used for address decoding. Each NRAM socket shall have machined pins and gold-plated contacts, and shall have its component identification permanently marked on the PCBA adjacent to the socket. EPROM sockets shall be a "Zero Insertion Force" Type. Sockets shall be:

3.1.11.1 For EPROM Socket:

28 pins	BR Intec Garry ZIF #06-00084, 3M OEM ZIP DIP #228-1296-00-3303 or equal
32 pins	3M OEM ZIP DIP #232-1297-00-3303 or equal

3.1.11.2 DIP (Dual Inline Package) Sockets shall have: An open frame design. Stamped beryllium copper, four-finger inner clip screw-machined brass receptacle sleeves. Glass-filled thermoplastic polyester insulator, rated UL94V-O. Current Rating 3 Amps. Plating: Sleeve, 10 micro inches, Contact , 30 micro inches.

AMP Type: xxx-AG10D or equal
Mill-Max Type 110-13-xxx-41-001 or equal

3.1.11.3 PLCC Sockets shall have an high temperature body/insulator rated UL94V-0. Phosphor bronze contacts with tin-over-nickel plating. Current rating, 1 Amp.

AMP PLCC socket-series HPT or equal
3M PLCC socket series PLCC-SMT or equal

3.1.12 If a Programmable device is used for address decoding and timing algorithms, the device code listing together with data sheet (s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the contractor uses to directly reproduce the device.

3.1.13 All circuit boards shall be coated with an insulating compound as specified in MIL-I-46058C Amendment 6. The insulating material shall have a fluorescent tracer added to facilitate examination by ultraviolet illumination.

3.1.14 ALL devices and components used in the design of the controller shall meet the temperature and electrical specifications outlined in this specification.

3.1.15 Use of extender boards shall not interfere with normal controller unit operation.

Section 2 ELECTRICAL

3.2.1 A 3-conductor cable a minimum of 3 feet in length shall supply the AC power to the controller unit. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

3.2.2 The front panel and chassis shall be connected to equipment ground.

3.2.3 The controller unit shall be unaffected by transient voltages normally experienced on commercial power lines. Refer to **1.8.5.1.5 above** (ELECTRICAL, ENVIRONMENTAL, AND TESTING).

3.2.3.1 At a minimum, Surge arrestors shall be provided between AC+, AC- and EG for protection against power line noise transients. The surge arrestors shall meet the following **minimum** requirements:

Recurrent peak voltage:	212 Volts
Energy rating maximum:	20 Joules
Power dissipation, average:	0.85 Watt
Peak current for pulses less than 6 Fsec:	2000 Amperes
Standby current:	Less than 1 mA

3.2.3.2 Two 0.5 ohm, 10 watt (**minimum**) wire-wound power resistors, shall be provided (1 on the AC+ power line and 1 on the AC- line) for protection of the surge arrestors.

3.2.3.3 Input and emission suppression shall be provided, across the AC+ and AC- power lines, by a CorCom 3S1A device or **equivalent and/or better**).

Section 3 170E-ATC CHASSIS :

3.3.1 **GENERAL**

3.3.1.1 The controller unit shall be designed to mount in a standard EIA 19-inch rack. Maximum height shall not exceed 7 inches.

3.3.1.2 The controller unit shall be housed in a compact, portable aluminum enclosure suitably protected against corrosion.

3.3.1.3 A permanent mechanical means shall be provided for each plug-in board or module, prevent accidental loosening due to vibration or transportation.

3.3.1.4 All printed circuit board modules shall be easily removable from the front of the controller unit, without the use of tools or disassembly of the controller chassis

3.3.1.5 All circuit boards (PCBAs) shall be vertically mounted.

3.3.1.6 **BOARD SPACING AND PLACEMENT**

3.3.1.6.1 Lateral spacing between boards shall be a minimum of 1.0 inch (25.4mm) from the PCBA surface to any component or surface of an adjacent board (PCBA).

3.3.1.6.2 Continuous nylon card guides, with ejectors, shall be provided for all internal PCBAs. Card guides shall be securely bonded to the chassis.

3.3.1.7 The four modem connectors shall be placed between the MCU board and the Power Supply.

Section 4 CONNECTORS

3.4.1 **General**

3.4.1.1 All circuit boards shall be pin compatible with the 170E-ATC Chassis and the 170E Chassis.

3.4.1.2 Connector C1S shall be mounted to allow access from the rear of the controller unit, and provide 44 inputs and 56 outputs of control interface to and from external devices or files.

3.4.1.3 (Optional) Connector C12S if provided, shall be located on the rear panel of the 170E-ATC chassis, between port C40 and I/O Port C1.

3.4.1.4 MODEM/UART CONNECTORS

3.4.1.4.1 The Model 400 Modems and MCU board UART Port connections into and out of the controller unit shall be made through Terminal Block T-1, and four 14 pin socket “M” Connectors (AMP 201298-1) mounted on the rear panel of the controller unit. Four DB9 socket connectors wired in parallel with the M connectors shall be mounted on the rear panel of the controller unit next to it's associated M connector.

3.4.1.4.2 The “M” connectors and the DB9 connectors shall be labeled C2S, C20S, C30S, and C40S.

3.4.1.5 The UART Port/MODEM Terminal Block T-1 and “M” Connectors shall have the following Pin Assignments (NOTE: All functions are in reference to a Modem’s perspective):

SIGNAL	T-1, UART Port 1, MODEM 1	C2s, UART Port 1, MODEM 1	C20s, UART Port 2, MODEM 2	C30s, UART Port 3, MODEM 3	C40s, UART Port 4, MODEM 4
AUDIO IN	1.	A.	A.	A.	A.
AUDIO IN	2.	B.	B.	B.	B.
AUDIO OUT	8.	C.	C.	C.	C.
AUDIO OUT	9.	E.	E.	E.	E.
+5VDC	N/A	D.	D.	D.	D.
CD	3.	H.	H.	H.	H.
RTS	4.	J.	J.	J.	J.
DATA IN	5.	K.	K.	K.	K.
DATA OUT	7.	L.	L.	L.	L.
CTS	6.	M.	M.	M.	M.
DC GND	10.	N.	N.	N.	N.
N.C.		F.	F.	F.	F.
N.C.		P.	P.	P.	P.
N.C.		R.	R.	R.	R.

Figure 3-1: T-1, C2, C20, C30 and C40 PIN ASSIGNMENTS

3.4.1.5.1 +5VDC shall be the only power supply voltage available on these connectors, and it shall be derived from a separate voltage regulator. (See Section 5 - Power Supply)

3.4.1.5.2 The maximum total current available to these connectors from the +5V power supply shall be limited to 300 mA.

3.4.1.6 The DB9 socket connectors shall have the following Pin Assignments:

SIGNAL	C2S, MODEM 1	C20S, MODEM 2	C30S, MODEM 3	C40S, MODEM 4
CD	1	1	1	1
DATA OUT	2	2	2	2
DATA IN	3	3	3	3
GND	5	5	5	5
RTS	7	7	7	7
CTS	8	8	8	8
N.C.	4	4	4	4
N.C.	6	6	6	6
N.C.	9	9	9	9

Figure 3-2: OPTIONAL UART Port/MODEM DB9 PIN ASSIGNMENTS

3.4.1.7 MODEM CONNECTORS

3.4.1.7.1 There shall be four modem connectors and interfaces. Modem slots one thru three shall be compatible with the Model 400 Dual Modem; and. Modem slot four shall be compatible with a Model 400 Single Modem.

3.4.1.8 Four PCB 22/44S Connectors shall be provided for the Model 400 Modules.

3.4.1.8.1 PCB 22/44 MODEM CONNECTOR PIN-OUTS:

MODEM CONNECTOR PIN	C2s, MODEM 1 SIGNAL	C20s, MODEM 2 SIGNAL	C30s, MODEM 3 SIGNAL	C40s, MODEM 4 SIGNAL
1	N.C.	N.C.	N.C.	N.C.
2	AUDIO IN 1+	AUDIO IN 2+	AUDIO IN 3+	AUDIO IN 4+
3	AUDIO IN 1-	AUDIO IN 2-	AUDIO IN 3-	AUDIO IN 4-
4	N.C.	N.C.	N.C.	N.C.
5	N.C.	N.C.	N.C.	N.C.
6	N.C.	N.C.	N.C.	N.C.
7	N.C.	N.C.	N.C.	N.C.
8	N.C.	N.C.	N.C.	N.C.
9	CD 2	CD 3	CD 4	N.C.
10	RTS 2	RTS 3	RTS 4	N.C.
11	DATA IN 2	DATA IN 3	DATA IN 4	N.C.
12	CTS 2	CTS 3	CTS 4	N.C.
13	DATA OUT 2	DATA OUT 3	DATA OUT 4	N.C
14	MISO	MISO	MISO	MISO
15	MOSI	MOSI	MOSI	MOSI
16	SCK	SCK	SCK	SCK
17	SS	SS	SS	SS
18	N.C.	N.C.	N.C.	GND
19	AUDIO OUT 2+	AUDIO OUT 3+	AUDIO OUT 4+	N.C.
20	AUDIO OUT 2-	AUDIO OUT 3-	AUDIO OUT 4-	N.C.
21	AUDIO IN 2+	AUDIO IN 3+	AUDIO IN 4+	N.C.
22	AUDIO IN 2-	AUDIO IN 3-	AUDIO IN 4-	N.C.
A	GND	GND	GND	GND
B	GND	GND	GND	GND
C	+12V COMM.	+12V COMM.	+12V COMM.	+12V COMM.
D	+12V COMM.	+12V COMM.	+12V COMM.	+12V COMM.
E	-12 VOLT	-12 VOLT	-12 VOLT	-12 VOLT
F	-12 VOLT	-12 VOLT	-12 VOLT	-12 VOLT
H	N.C.	N.C.	N.C.	N.C.
J	N.C.	N.C.	N.C.	N.C.
K	CD 1	CD 2	CD 3	CD 4
L	RTS 1	RTS 2	RTS 3	RTS 4
M	DATA IN 1	DATA IN 2	DATA IN 3	DATA IN 4
N	CTS 1	CTS 2	CTS 3	CTS 4
P	DATA OUT 1	DATA OUT 2	DATA OUT 3	DATA OUT 4
R	MISO	MISO	MISO	MISO
S	MOSI	MOSI	MOSI	MOSI
T	SCK	SCK	SCK	SCK
U	SS	SS	SS	SS
V	GND	N.C.	GND	N.C.
W	N.C.	GND	GND	N.C.
X	AUDIO OUT 1+	AUDIO OUT 2+	AUDIO OUT 3+	AUDIO OUT 4+
Y	AUDIO OUT 1-	AUDIO OUT 2-	AUDIO OUT 3-	AUDIO OUT 4-
Z	N.C.	N.C.	N.C.	N.C.

NOTES:
Modem Slot 1 supports UART Port 1 and 2.
Modem Slot 2 supports UART Port 2 and 3.
Modem Slot 3 supports UART Port 3 and 4.
Modem Slot 4 supports UART Port 4.
The Motorola SPI serial buss is wired across all four slots.

Figure 3-3: PCB 22/44S MODEM CONNECTOR PIN OUTS

3.4.1.9 Ribbon Cables, if used, shall terminate with properly rated and easily repairable connectors. If specialized tools are required to repair the supplied ribbon cables; two (2) sets of such tools shall be provided. The ribbon cables shall be dressed in a neat and orderly fashion to avoid sharp bends.

Section 5 POWER SUPPLIES

3.5.1 A power supply shall be provided to produce all DC power necessary to operate the controller unit. The power supply shall be modular and easily removable from the chassis.

3.5.2 Power Supply design shall be such that all components are operated at or below 80 percent of their maximum ratings.

3.5.3 Voltage regulators shall comply to the following specifications over a line voltage range of 90VAC to 135VAC:

REGULATION	CURRENT (min)	RIPPLE AND NOISE (max)
+ 5 ("0.10V) (Logic)	2.4A	100mV P-P
+ 5 ("0.25V) (C2, C20, C30, C40)	300mA	100mV P-P
+12 ("0.60V)	1.0A	100mV P-P
-12 ("0.60V)	500mA	100mV P-P
- 5 ("0.25V) required only if needed for the controller to operate.	400mA	100mV P-P

Figure 3-4: VOLTAGE REGULATION

3.5.4 If regulated +5V is required for the Display Module, a separate regulator shall be used.

3.5.5 Test points shall be provided for monitoring all power supply voltages. All test points shall be clearly labeled and readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 0.0625 inch (1.59mm) diameter and 0.1875 inch (4.76mm) high, minimum. The clearance between test points and other components shall be 0.25-inch (6.35mm), minimum.

3.5.6 The DC ground shall not be connected to equipment ground.

3.5.7 Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ("17) msec after the NMI line goes LOW.

3.5.8 The maximum DC voltage generated shall not exceed 45 volts.

3.5.9 The Power Supply shall be designed so that all required filtering and regulation be achieved within the power supply module

3.5.10 **STANDBY POWER:** A stored-capacitance type device shall be provided in lieu of a battery. This device shall be used to power **ONLY** the Down Time Accumulator (DTA) circuit, and be of sufficient capacity to operate the DTA for a minimum of 8 hours, while the controller unit is powered down.

Section 6 MOTHERBOARD and BUS SYSTEM

3.6.1.1 All circuit boards shall be pin compatible with the 170E-ATC Chassis and the 170E Chassis.

3.6.2 **SYSTEM MEMORY MAPS (with Type ATC-HC11 MCU BOARD) .**

MAP	BANK 2	BANK 1	MEMORY/SIZE	STANDARD ADDRESS
1	HIGH	HIGH	NRAM (28K)	0000-6FFF
			MCU REGISTERS (96 BYTES)	7000-705F
			VOLATILE CPU RAM (928 BYTES)	7060-73FF
			I/O and CONTROL (511 BYTES)	7400-75FF
			NRAM 2K	7600-7FFF
		(1)xxxx	PROM 32K	(1)8000-(1)FFFF

MAP	BANK 2	BANK 1	MEMORY/SIZE	STANDARD ADDRESS
2	HIGH	LOW	NRAM 28K	0000-6FFF
			MCU REGISTERS (96 BYTES)	7000-705F
			VOLATILE CPU RAM (928 BYTES)	7060-73FF
			I/O and CONTROL (511 BYTES)	7400-75FF
			NRAM 2K	7600-7FFF
		(0)xxxx	PROM 32K	(0)8000-(0)FFFF

MAP	BANK 2	BANK 1	MEMORY/SIZE	STANDARD ADDRESS
3	LOW	HIGH	NRAM 8K	0000-1FFF
		(1)xxxx	PROM 20K	(1)2000-(1)5FFF
			NRAM 4K	6000-6FFF
			MCU REGISTERS (96 BYTES)	7000-705F
			VOLATILE CPU RAM (928 BYTES)	7060-73FF
			I/O and CONTROL (511 BYTES)	7400-75FF
			NRAM 2K	7600-7FFF
		(1)xxxx	PROM 32K	(1)8000-(1)FFFF

MAP	BANK 2	BANK 1	MEMORY/SIZE	STANDARD ADDRESS
4	LOW	LOW	NRAM 8K	0000-1FFF
		(0)xxxx	PROM 20K	(0)2000-(0) 5FFF
			NRAM 4K	6000-6FFF
			MCU REGISTERS (96 BYTES)	7000-705F
			VOLATILE CPU RAM (928 BYTES)	7060-73FF
			I/O and CONTROL (511 BYTES)	7400-75FF
			NRAM 2K	7600-7FFF
		(0)xxxx	PROM 32K	(0)8000-0FFFF
BANK 1 IS MCU PORT G BIT 0 OUTPUT BANK 2 IS MCU PORT G BIT 1 OUTPUT AFTER RESET, THE STATE OF BANK 1 IS HIGH AND BANK 2 IS LOW (MAP 3).				

Figure 3-5: ATC-HC11 SYSTEM MEMORY MAPS

3.6.3 **I/O and CONTROL ADDRESS MAP (with Type ATC-HC11 MCU BOARD)**

ADDRESS RANGE	FUNCTION	BYTES USED
7400	DTA RESET (WRITE)	1
7400	DTA MINUTES (READ)	1
7401-740A	I/O	10
7404, bit 1	RESTART ORIENTATION TIMER (READ)	"
740B-740E	NOT USED	4
740F	DTA SECONDS (READ)	--
7410-741F	RESERVED	16
7420-7427	ST16C654 QUAD UART PORT A INTERNAL REGISTERS	8
7428-742F	ST16C654 QUAD UART PORT B INTERNAL REGISTERS	8
742F-7437	ST16C654 QUAD UART PORT C INTERNAL REGISTERS	8
7438-743F	ST16C654 QUAD UART PORT D INTERNAL REGISTERS	8
7440-74FF	RESERVED	192
7500-75FE	RESERVED	
75FF	RTC RESET (WRITE)	1
75FF	IRQ STATUS PORT (READ)	"
" " Bit 1	UART IRQ STATUS BIT	"
" " Bit 2	RESERVED	"
" " Bit 3	RESERVED	"
" " Bit 4	RESERVED	"
" " Bit 5	BANK 2 STATUS BIT	"
" " Bit 6	BANK 1 STATUS BIT	"
" " Bit 7	DTA MAXOUT STATUS BIT:	"
" " Bit 8	RTC IRQ STATUS BIT	"
X7600-X7FF7	MCU BOARD NRAM	512
7FF8-7FFF	NRAM REAL-TIME CLOCK/CALENDAR REGISTERS	8
(0)8000 – (0)FFFF	TRAFFIC SIGNAL EPROM	32K*
(1)8000 – (1)FFFF	TRAFFIC SIGNAL EPROM	32K*
(0)XXXX = BANK 1 is LOW (1)XXXX = BANK 1 is HIGH		

Figure 3-6: ATC-HC11 GENERAL SYSTEM ADDRESS MAP

3.6.4 **I/0 AND MEMORY SYSTEM BUSSES –**

3.6.4.1 As there is no Memory Module in the 170E-ATC chassis, there is no off board Memory Buss. The I/O Buss is the same as the 170E.

3.6.5 **INPUT & OUTPUT INTERFACES** shall utilize ground-true logic. The transfer of data between interface and working registers within the CPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of CPU read/write command at the time the given address is valid.

3.6.5.1 **OUTPUT INTERFACE:** The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MCU. This interface shall provide an open

collector output capable of sinking up to 100 mA at 40 VDC. A "1" from the MCU shall be presented as a grounded collector, and a "0"' presented as an open circuit. Once a port is written, the data shall remain present and stable either until another word is written into it or until the power is turned off.

3.6.5.2 The state of these output ports at the time of power up, or below power failure threshold, shall be an open circuit.

3.6.5.3 **OUTPUT ADDRESS MAP**:

OUTPUT PORT	ADDRESS	BIT	FUNCTION/ OUTPUT PIN	OUTPUT PORT	ADDRESS	BIT	FUNCTION/ OUTPUT PIN
1	7401	1	C1 – 2	6	7406	1	C1 – 83
		2	C1 – 3			2	C1 – 84
		3	C1 – 4			3	C1 – 85
		4	C1 – 5			4	C1 – 86
		5	C1 – 6			5	C1 – 87
		6	C1 – 7			6	C1 – 88
		7	C1 – 8			7	C1 – 89
		8	C1 – 9			8	C1 – 90
2	7402	1	C1 – 10	7	7407	1	C1 – 91
		2	C1 – 11			2	C1 – 93
		3	C1 – 12			3	C1 – 94
		4	C1 – 13			4	C1 – 95
		5	C1 – 14			5	C1 – 96
		6	C1 – 15			6	C1 – 97
		7	C1 – 16			7	C1 – 98
		8	C1 – 17			8	C1 – 99
3	7403	1	C1 – 19	8	7408	1	Character control, PHASE
		2	C1 –20			2	Character control, INTERVAL
		3	C1 – 21			3	Character control, TIMING, LS
		4	C1 – 22			4	Character control, TIMING, NLS
		5	C1 – 23			5	Character control, TIMING, NMS
		6	C1 – 24			6	Character control, TIMING, MS
		7	C1 – 25			7	Call Light 8
		8	C1 – 26			8	Call Light 9
4	7404	1	C1 – 27	9	7409	1	Character, LS
		2	C1 – 28			2	Character, NLS
		3	C1 – 29			3	Character, NMS
		4	C1 – 30			4	Character, MS
		5	C1 – 31			5	Decimal Point
		6	C1 – 32			6	Blanking, PHASE and INTERVAL
		7	C1 – 33			7	Blanking, TIMING
		8	C1 – 34			8	--
5	7405	1	C1 – 35	A	740A	1	Call Light 0
		2	C1 – 36			2	Call Light 1
		3	C1 – 37			3	Call Light 2
		4	C1 – 38			4	Call Light 3
		5	C1 – 100			5	Call Light 4
		6	C1 – 101			6	Call Light 5
		7	C1 – 102			7	Call Light 6
		8	C1 – 103			8	Call Light 7

Figure 3-7: OUTPUT ADDRESS MAP

3.6.5.4 **INPUT INTERFACE** The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5VDC,

shall be turned OFF (false) when the input current is less than 100 mA or the input voltage exceeds 8.5 VDC. Floating or unused inputs shall be pulled up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MCU. Ground on any input shall be interpreted by the MCU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MCU when that input is read.

3.6.5.4.1 **INPUT ADDRESS MAP** (READ):

INPUT PORT	170E-ATC ADDRESS	BIT	FUNCTION INPUT PIN	INPUT PORT	170E-ATC ADDRESS	BIT	FUNCTION INPUT PIN
1	7401	1	C1 – 39	5	7405	1	C1 – 67
		2	C1 – 40			2	C1 – 68
		3	C1 – 41			3	C1 – 69
		4	C1 – 42			4	C1 – 70
		5	C1 – 43			5	C1 – 71
		6	C1 – 44			6	C1 – 72
		7	C1 – 45			7	C1 – 73
		8	C1 – 46			8	C1 – 74
2	7402	1	C1 – 47	6	7406	1	C1 – 75
		2	C1 – 48			2	C1 – 76
		3	C1 – 49			3	C1 – 77
		4	C1 – 50			4	C1 – 78
		5	C1 – 51			5	C1 – 79
		6	C1 – 52			6	C1 – 80
		7	C1 – 53			7	C1 – 81
		8	C1 – 54			8	C1 – 82
3	7403	1	C1 – 55	7	7407	1	Keypad Contact
		2	C1 – 56			2	Keypad Char LS
		3	C1 – 57			3	Keypad Char NLS
		4	C1 – 58			4	Keypad Char NMS
		5	C1 –59			5	Keypad Char MS
		6	C1 – 60			6	Stop Time Switch
		7	C1 – 61			7	--
		8	C1 – 62			8	--
4	7404	1	Restart Timer	8	7408	1	--
		2	--			2	--
		3	--			3	--
		4	--			4	--
		5	C1 – 63			5	--
		6	C1 – 64			6	--
		7	C1 – 65			7	--
		8	C1 – 66			8	--

Figure 3-8: INPUT ADDRESS MAP

3.6.6 **DATA AND ADDRESS BUS REQUIREMENTS**

3.6.6.1 All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 nsec.

3.6.6.2 All Address Bus Inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 picofarads.

Section 7 CIRCUIT BOARDS

3.7.1 **GENERAL**

3.7.1.1 The Model 170E-ATC Controller Unit shall be modular in design. All Printed Circuit Boards (PCBAs) shall be vertically mounted.

3.7.1.2 All circuit boards shall be pin compatible with the 170E-ATC Chassis and the 170E Chassis.

3.7.1.3 All circuit boards shall be of *two*-layer design.

3.7.1.4 All boards shall be uniquely keyed.

3.7.1.5 The motherboard shall have connectors with molded keys.

3.7.1.6 The Model 170E-ATC Controller Unit shall consist of the following:

170E-ATC Chassis
ATC-HC11 MCU Board
Type 170E Input Board
Type 170E Output Board
Display Board (optional)
Unit Power Supply with external power connection
Type 170E Front Panel Assembly
Internal System Interface (Motherboard)
Connectors C1S, C2S, C20S, C30S, C40S, and T-1
Provisions for 4 Model 400 compatible DUAL MODEMS

3.7.1.7 The composition weight shall not exceed 25 pounds (11.3 kg).

3.7.2 **CPU /MCU BOARDS, GENERAL**

3.7.2.1 **NON-MASKABLE INTERRUPT** (NMI**):** The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the MCU NMI line to immediately go LOW. The line shall remain LOW until the RES goes LOW, to prevent multiple NMI issuances.

3.7.2.2 **RESET INTERRUPT (RES):** The RES is exclusively assigned to Power Restoration and MCU Startup. The RES line shall go LOW 3 (±1) msec following the NMI going LOW. The line shall remain LOW until 150 ("75) msec after Power Restoration.

3.7.2.3 **INTERRUPT REQUEST (IRQ)** The IRQ Line shall be jointly used by the RTC and UART PORTS to initiate IRQ to the MCU.

3.7.2.4 **REAL TIME CLOCK (RTC):**. Real Time Clock Circuitry shall be provided to trigger an interrupt to the MCU on the IRQ line, and set bit 8 of the Status byte, **ONLY** once every 1/60 of a second, during the 270 degree to 330 degrees portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120VAC 60 Hz frequency.

3.7.3 **MODEL 170 ATC HC11 MCU BOARD :** The ATC-HC11 MCU PCBA shall use a MC68HC11F1 MCU, a ST16C654 QUAD UART and a DS1744 Nonvolatile Timekeeping RAM.

3.7.3.1.1 **MCU CLOCK TIMING:** Clock circuitry shall be provided to generate the MCU clock timing.

3.7.3.1.1.1 The MCU clock circuitry shall be located within 2 inches (50.8MM) of the MCU clock input pins.

3.7.3.1.1.2 The MCU clock frequency shall be 9.8304 MHz. Note, if in the future the MCU frequency is changed, it shall not affect the UART clock frequency or baud rates.

3.7.3.2 **MC68HC11F1 MCU CONFIG REGS and RAM**. At power on the INIT Register should be set to $77 (77 Hex) to map the MCU internal registers and internal volatile RAM to the 7xxx block of memory. Refer to Motorola's MC68HC11F1 Technical Data for more detail.

ADDRESS[1]	BIT 7	6	5	4	3	2	1	BIT 0	FUNCTION
$7000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$7001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$7002	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$7003	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$7004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$7005	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PORTF
$7006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$7007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$7008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$7009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$700A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$700B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$700C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$700D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$700E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$700F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$7010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$7011	Bit 7	6	5	4	3	2	1	bit 0	TIC1 (Low)
$7012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$7013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$7014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$7015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$7016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (High)
$7017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$7018	Bit 15	14	13	12	11	10	9	Bit 0	TOC2 (High)
$7019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$701A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$701B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$701C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$701D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$701E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (High)
$701F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Low)
$7020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$7021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$7022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$7023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$7024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$7025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$7026	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0	PACTL
$7027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$7028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$7029	SPIF	WCOL	0	MODF	0	0	0	Bit 0	SPSR
$702A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$702B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$702C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$702D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$702E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$702F	Bit 7	6	5	4	3	2	1	Bit 0	SCDR
$7030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$7031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$7032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2

[1] Address is $7xxx after the MPU internal register INIT is set to $77.

$7033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$7034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$7035	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$7036									Reserved
$7037									Reserved
$7038	GWOM	CWOM	CLK4X	0	0	0	0	0	OPT2
$7039	ADPU	CSEL	IRQE	DLY	CME	FCME	CR1	CR0	OPTION
$703A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$703B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
$703C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$703D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$703E	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	0	TEST1
$703F	EE3`	EE2	EE1	EE0	1	NOCOP	1	EEON	CONFIG
$7040 to $705B									Reserved Reserved
$705C	IO1SA	IO1SB	IO2SA	IO2SB	GSTHA	GSTHB	PSTHA	PSTHB	CSSTRH
$705D	IO1EN	IO1PL	IO2EN	IO2PL	GCSPR	PCSEN	PSIZA	PSIZB	CSCTL
$705E	GA15	GA14	GA13	GA12	GA11	GA10	0	0	CSGADR
$705F	IO1AV	IO2AV	0	GNPOL	GAVLD	GSIZA	GSIZB	GSIZC	CSGSIZ
$7060 to $73FF									VOLATILE MCU RAM

Figure 3-9: MC68HC11F1 CONFIG REGS and RAM

3.7.3.3 **QUAD UART:** AN EXAR ST16C654 QUAD UART IC with 64-BYTE FIFO or a code compatible IC shall be provided for serial data communications. The QUAD UART shall be used with Motorola Data Buss (68 Mode) Interconnections. Refer to ST16C654 Data Sheet for more details.

3.7.3.3.1 UART INTERNAL REGISTERS: Refer to ST16C654 Data Sheet for more details.

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Div Latch High Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7] = 0
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	LCR[7] = 0
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	LCR[7] = 0
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR[7] = 0
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	LCR = 0xBF
1 0 1	Xon-2 - Xon Character 2	Read/Write	LCR = 0xBF
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	LCR = 0xBF
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	LCR = 0xBF
X X X	FSTAT - FIFO Status Register	Read-only	FSRS# pin is logic 0

Table 3-1 UART CHANNEL A AND B UART INTERNAL REGISTERS

3.7.3.3.2 QUAD UART CLOCK: Clock circuitry shall be provided to generate the MCU clock timing. The QUAD UART clock frequency shall be 9.8304 MHz.

3.7.3.3.3 BAUD RATES: All UART ports shall work at the following baud rates:

BAUD RATES
1200 Baud
2400 Baud
4800 Baud
9600 Baud
19.2K Baud
38.4K Baud
76.8K Baud
153.6K Baud

Figure 3-10: UART. BAUD RATES

3.7.3.4 The Baud Rate shall be independently selectable for each UART Port by software.

3.7.3.5 **DOWNTIME ACCUMULATOR (DTA):**

3.7.3.5.1 A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon Power Failure and continue counting until the RES line goes HIGH following Power Restoration.

3.7.3.5.2 The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ±250 msec over the 255-minute range. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and the Seconds Register reset to "0". When the Minutes reach 255, the DTA MAXOUT bit (bit 7) of the Status Byte shall be set, and the DTA shall stop counting.

3.7.3.5.3 Once the Minutes Register reaches maximum count, it shall remain latched in this condition until reset by software following Power Restoration.

3.7.3.5.4 All DTA circuitry, including the Unit Standby Power source, shall be located on one board.

3.7.3.6 **RESTART TIMER**: A Restart Timer Circuit shall be provided to react to the duration of power outage. The Restart Timer output state is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (±0.25) seconds, its output state shall go to LOW and remain in that state for 50 (±24) msec after the RES line goes HIGH. If power is restored prior to the timer, timing out, the output shall remain HIGH and the timer shall be reset to "0".

3.7.3.7 **MODEM AND UART PORT REQUIREMENTS**

3.7.3.7.1 The interface between the UART Ports and the MODEMS shall comply with EIA RS-232-C Standards. The RTS and TX DATA lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12VDC respectively.

3.7.3.7.2 There shall be four modem connectors and interfaces. Modem slots one thru three shall be compatible with the Model 400 Dual Modem, and Modem slot four with the MCU Model 400 Single Modem.

3.7.3.7.3 The first modem connector and interface, compatible with the Model 400 Dual Modem, and two UART Ports, designated as UART Port #1 and #2, shall be provided. Connections into and out of the controller unit shall be made through Connector C2S, C20S. The control and data transmission lines from Connector C2S shall be paralleled through Terminal Block T-1 (TYPE T Connector).

3.7.3.7.4 The second modem connector and interface, compatible with the Model 400 Dual Modem, and two UART Ports, designated as UART Port #2 and #3, shall be provided, with access via connectors C20S and C30S.

3.7.3.7.5 The third modem connector and interface, compatible with the Model 400 Dual Modem, and two UART Ports, designated as UART Port #3 and #4, shall be provided, with access via connectors C30S and C40S.

3.7.3.7.6 The fourth modem connector and interface, compatible with the Model 400 Single Modem, and one UART Port, designated as UART Port #4, shall be provided, with access via connector C40S.

3.7.3.7.7 The C2S, C20S, C30S, and C40S connectors shall all be mounted on the rear panel of the controller.

3.7.4 **Model 170E CPU BOARD:**

3.7.4.1 The Model 170E CPU Board shall be able to operate normally if installed in a 170E-ATC Chassis (with EPROM and NRAM on the CPU Board.

3.7.5 **CONNECTORS for ATC FRONT PANEL and FRONT PANEL UART PORT 4 (C50):**

3.7.5.1.1.1 These serial ports are needed to interface with the optional ATC (Type 2070) Front Panel. All interface buffers from the MCU to the Front Panel shall be RS422 and converted to RS232 format as required on the front panel board.

3.7.5.1.1.2 A 14 pin, Low Profile Box Header Connector and circuitry shall be provided to support the ATC Front Panel C50 serial port. The pin-out shall be:

HEADER PIN	SIGNAL	HEADER PIN	SIGNAL
1	C50 RXD -	8	FP TXD -
2	C50 RXD +	9	/RESET
3	C50 TXD +	10	PORT4 CONT
4	C50 RXD -	11	FP ACTIVE LED
5	FP RXD -	12	DC COMM
6	FP RXD +	13	DC COMM
7	FP TXD +	14	DC COMM

Figure 3-11: ATC FRONT PANEL SERIAL PORT

3.7.5.1.1.3 UART Serial Port 4 will be routed to the front panel RS232 connector (C50), , when a serial cable is plugged into the front panel RS232 connector that has pin 1 tied to DC COMM. This signal, C50 Enable, when grounded, will switch port 4 from C40 to C5; otherwise, it is routed to the controller rear panel (C40).

3.7.5.2 There shall be one LED indicator, located on the front of the MCU board, which shall be controlled via a software output of Port G bit 3.

3.7.5.3 The +5VDC, +12VDC and -12 VDC voltages input to the MCU board shall have TransZorb® protection.

3.7.6 The **INPUT BOARD** shall contain only the 170E controller input circuitry (and the DTA if it is not on the MCU board).

3.7.7 The **OUTPUT BOARD** shall contain only the 170E controller output circuitry.

3.7.8 The **OPTIONAL DISPLAY BOARD** shall contain only the circuitry needed to run the front panel display and keyboard.

Section 8 FRONT PANEL (See Section 11)

3.8.1 The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous stainless steel or aluminum piano hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

3.8.2 An approved latch mechanism shall be provided to secure the right side of the front panel to the chassis.

3.8.3 The front panel shall be electrically connected by means of Connector C3.

3.8.4 The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 0.40-inch high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the MCU through the output interface to the display shall result in the display of each character in its non-inverted state.

3.8.5 The front panel shall be provided with 10 LED indicators, labeled "CALL/ACTIVE" and numbered "0" through "9" to the right or left of each indicator.

3.8.6 The front panel MAY include an LED indicator displaying the "Watchdog" output, labeled same or "WDT". The "Battery Charging" LED indicator no longer required may be used for this purpose.

3.8.7 A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MCU shall result in each character being received in its non-inverted state. The character shall consist of 4 bits of binary data, while the character control shall consist of 1 bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 0.075 square inch and shall be mounted on a minimum of 0.50-inch center; shall have an actuation threshold between 50 and 100 grams and shall provide a positive tactical indication of contact. Key contacts shall have design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 msec following contact opening.

3.8.8 The front panel shall be provided with a toggle switch to enable the stop timing function and shall be labeled "STOP TIMING".

3.8.9 An AC POWER toggle switch and fuse shall be provided. The switch and fuse shall protrude through the front panel, but not be attached (it shall remain with the modular Power Supply when the front panel is opened or removed). The fuse shall be a 3AG Type rated at 150% of unit load.

Section 9 DIAGNOSTIC AIDS

3.9.1 Extender Boards, wrap-around cables, and test jigs shall be available from the manufacturer, at the time of equipment purchase, and in quantities determined at the time of purchase.

3.9.2 The Contractor shall furnish a Diagnostic Test Program, resident in the provided EPROM, in each controller unit, at the time of delivery. The Program shall test and report failures on all functions and circuits within the 170E and/or 170E-ATC controller. This Program shall meet the following requirements.

3.9.3 Five copies of a 170E-ATC Diagnostic Test Program Software Manual shall be supplied. The Manual shall include full and complete documentation of test procedures, including, but not limited to the following:

170E-ATC Verification Test Operation
Individual Diagnostic Tests
Program listings in assembly format, with detailed comments
Detailed flow charts, which are keyed to the software listing using instruction labels and subroutine names.

3.9.4 The Diagnostic Test Program shall be an integrated Front Panel and CRT/Keyboard program.

3.9.5 The Diagnostic Test Program shall include, but not be limited to, the following capabilities:

Display Test Results
Display Number of Test Performed
Display Accumulated Number of Test Failed
Display Start Up Test Results
Automatic Cyclic Test
Manual Test Selection and Repeat of a Single Test (loop)
UART Port #1 with and without Modem
UART Port #2 with and without Modem
UART Port #3 with and without Modem
UART Port #4 with and without Modem

3.9.5.1 START-UP TESTS:

RAM Identify - size and address
RAM Pretest
RAM Retention
Number of NMI's
Number of Resets
Restart Timer
DTA Display

3.9.5.2 AUTOMATIC TESTS:

RAM Short
RAM Extensive
Memory Mapping and Addressing
I/O Wrap-Around
Real Time Clock
Display
Keyboard
UART Port #1 with and without Modem
UART Port #2 with and without Modem
UART Port #3 with and without Modem
UART Port #4 with and without Modem
MCU Instruction
System Addressing
EPROM Checksum

3.9.6 The Diagnostic Program, when performing the Input/Output wrap-around test, shall incorporate the Input Port/Output Port addressing as specified in Table 1-1.

3.9.7 The C1 wrap-around connector shall be wired as specified below:

C1 WRAP-AROUND CONNECTOR PIN-OUT											
JUMPER						JUMPER					
FROM C1 OUTPUT			TO C1 INPUT			FROM C1 OUTPUT			TO C1 INPUT		
PIN	PORT	BIT	PIN	PORT	BIT	PIN	PORT	BIT	PIN	PORT	BIT
2	01	1	39	01	1	35	05	1	67	05	1
3		2	40		2	36		2	68		2
4		3	41		3	37		3	69		3
5		4	42		4	38		4	70		4
6		5	43		5	100		5	71		5
7		6	44		6	101		6	72		6
8		7	45		7	102		7	73		7
9		8	46		8	103		8	74		8
10	02	1	47	02	1	83	06	1	75	06	1
11		2	48		2	84		2	76		2
12		3	49		3	85		3	77		3
13		4	50		4	86		4	78		4
15		5	51		5	87		5	79		5
16		6	52		6	88		6	80		6
17		7	53		7	89		7	81		7
18		8	54		8	90		8	82		8
19	03	1	55	03	1	91	07	1	75	06	1
20		2	56		2	93		2	76		2
21		3	57		3	94		3	77		3
22		4	58		4	95		4	78		4
23		5	59		5	96		5	79		5

24		6	60		6	97		6	80		6
25		7	61		7	98		7	81		7
26		8	62		8	99		8	82		8
27	04	1	55	03	1						
28		2	56		2						
29		2	57		3						
30		4	58		4						
31		5	59		5	1	LOGIC GND	5	63	04	5
32		6	60		6	14	LOGIC GND	6	64		6
33		7	61		7	92	LOGIC GND	7	65		7
34		8	62		8	104	LOGIC GND	8	66		8

Figure 3-12: C1 WRAP-AROUND CONNECTOR PIN-OUT

3.9.8 The C2, C20, C30, and C40 wrap-around connectors (with Modem) shall be wired as specified below:

C2, C20, C30, C40 WRAP-AROUND (MODEM) CABLE WIRE LIST			
From Pin	Function	To Pin	Function
A	Audio In	C	Audio Out
B	Audio In	E	Audio Out
NOTE: Audio In / Audio Out - refers to In/Out of a MODEM			

Figure 3-13: MODEM WARP-AROUND

3.9.9 The C2, C20, C30, and C40 wrap-around connectors (without Modem) shall be wired as specified below:

C2, C20, C30, C40 WRAP-AROUND (UART) CABLE WIRE LIST			
From Pin	Function	To Pin	Function
J	RTS	M	CTS
J	RTS	H	DCD
K	DATA IN	L	DATA OUT
NOTE: Data In / Data Out - refers to In/Out of a MODEM.			

Figure 3-14: C2, C20, C30, C40 WRAP-AROUND (UART) CABLE WIRE LIST

Section 10 MODEL 400 MODEM MODULE

3.10.1 The MODEM shall provide two-wire half-duplex and four-wire full duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN/OUT.

3.10.2 The MODEM shall be compatible with Bell Standard 202S and comply with the following requirements:

3.10.2.1 **DATA RATE**: 300 to 1200 baud modulation.

3.10.2.2 **MODULATION:** Phase coherent frequency shift keying (FSK).

3.10.2.3 **DATA FORMAT:** Asynchronous, serial by bit.

3.10.2.4 **LINE AND SIGNAL REQUIREMENTS:** Type 3002 voice-grade, unconditioned.

3.10.2.5 **UART Port and MODEM INTERFACE:** EIA RS-232-C standards.

3.10.2.6 **TONE CARRIER FREQUENCIES** (Transmit & Receive)**:** 1200 Hz (MARK) and 2200 Hz (SPACE) with ±1% tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

3.10.2.7 **TRANSMITTING OUTPUT SIGNAL LEVEL:** 0, -2, -4, -6, and -8 dBm (at 1700 Hz) continuous or switch selectable.

3.10.2.8 **RECEIVER INPUT SENSITIVITY:** 0 to -40 dBm.

3.10.2.9 **RECEIVER BAND PASS FILTER:** Shall meet the error rate requirement specified in Paragraph 2.10.2.15 and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

3.10.3 **CLEAR-TO-SEND (CTS) DELAY:** 12 ("2) msec.

3.10.3.1 **RECEIVE LINE SIGNAL DETECT TIME:** 8 ("2) msec mark frequency.

3.10.3.2 **RECEIVE LINE SQUELCH:** 6.5 ("1) msec, 0 msec (OUT).

3.10.3.3 **SOFT CARRIER (900 Hz) TURN OFF TIME:** 10 ("2) msec.

3.10.3.4 **MODEM RECOVERY TIMER:** Capable of receiving data within 22 msec after completion of transmission.

3.10.3.5 **ERROR RATE:** Shall not exceed 1 bit in 100,000 bits, with a signal- to-noise ration of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

3.10.3.6 **TRANSMIT NOISE:** Less than 50 dB across 600 ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

3.10.3.7 The MODEM power requirements are as follows:

Input Voltages	Maximum Current Consumption
+12 VDC	75 mA
-12 VDC	75 mA

Figure 3-15: MODEM POWER REQUIREMENTS

3.10.3.8 Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data

3.10.3.9 Dual Modem Pin-out

TABLE 3-3MODEL 400 DUAL MODEM PIN-OUT			
Pin	Function	Pin	Function
2	Modem 1 AUDIO IN	A	DC GROUND
3	Modem 1 AUDIO IN	B	DC GROUND
9	UART Port 2 DCD	C	+12 VDC
10	UART Port 2 RTS	D	+12 VDC

11	UART Port 2 DATA IN	E	-12 VDC
12	UART Port 2 CTS	F	-12 VDC
13	UART Port 2 DATA OUT	K	UART Port 1 DCD
19	Modem 2 AUDIO OUT	L	UART Port 1 RTS
20	Modem 2 AUDIO OUT	M	UART Port 1 DATA IN
21	Modem 2 AUDIO IN	N	UART Port 1 CTS
22	Modem 2 AUDIO IN	P	UART Port 1 DATA OUT
		X	Modem 1 AUDIO OUT
		Y	Modem 1 AUDIO OUT

Figure 3-16: MODEL 400 DUAL MODEM PIN-OUT

Section 11 CHAPTER DETAILS

3.11.1 TYPE 170E-ATC FRONT PANEL

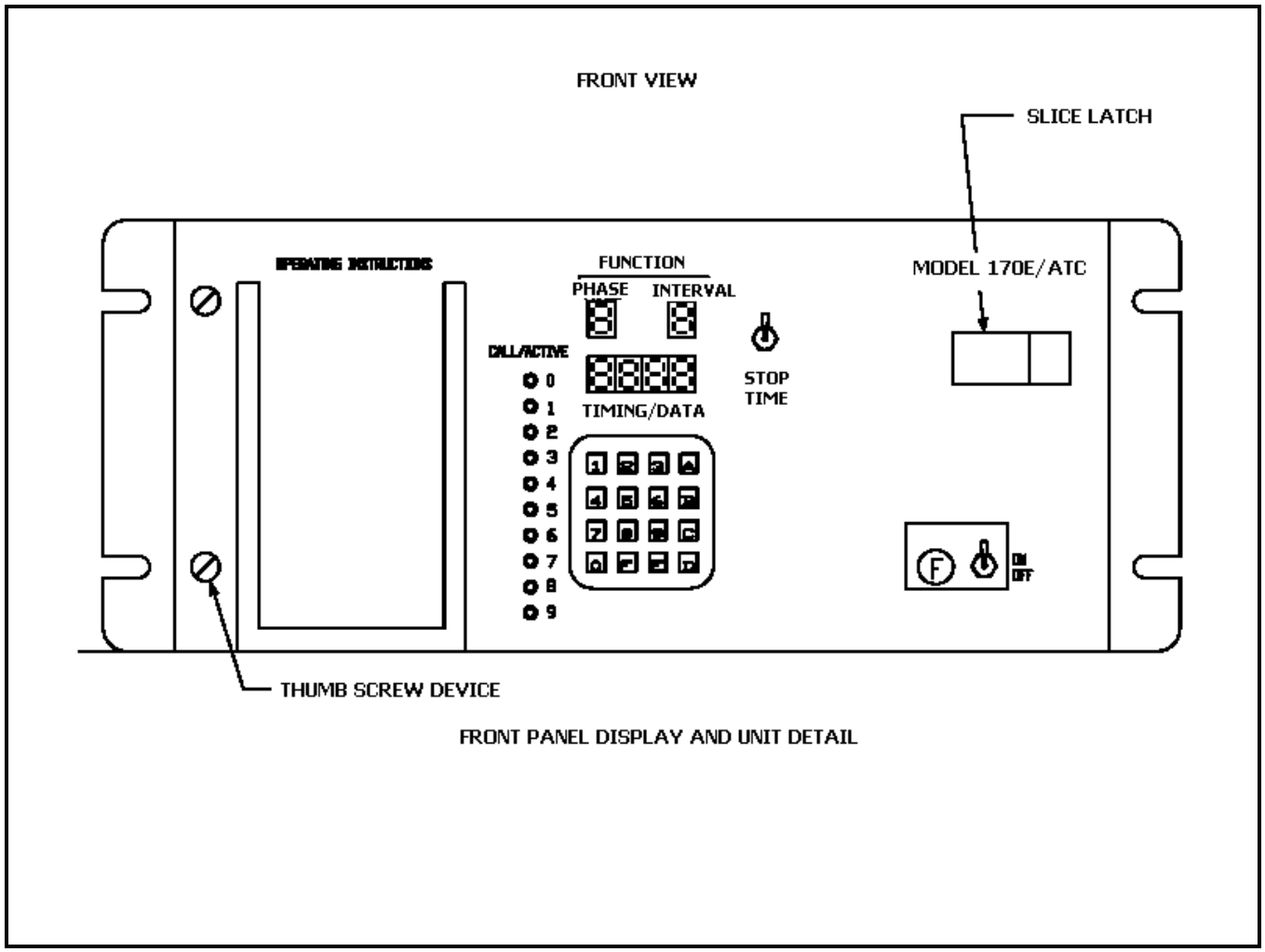


Figure 3-17: TYPE 170E-ATC FRONT PANEL

3.11.2 TYPE 170-ATC FRONT PANEL

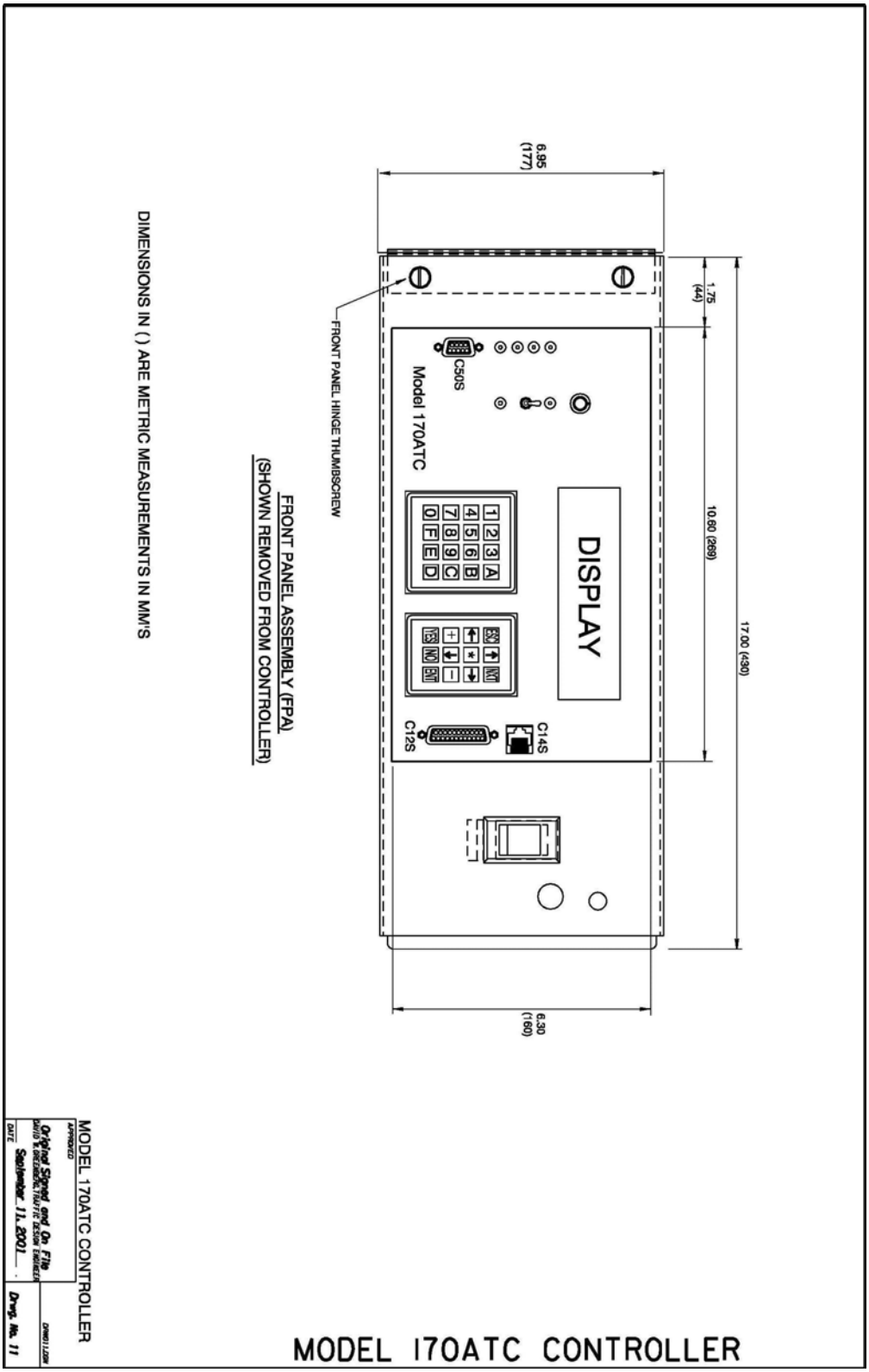


Figure 3-18: TYPE 170-ATC FRONT PANEL (OPTIONAL)

3.11.3 MODEL 170E-ATCBLOCK DIAGRAMS

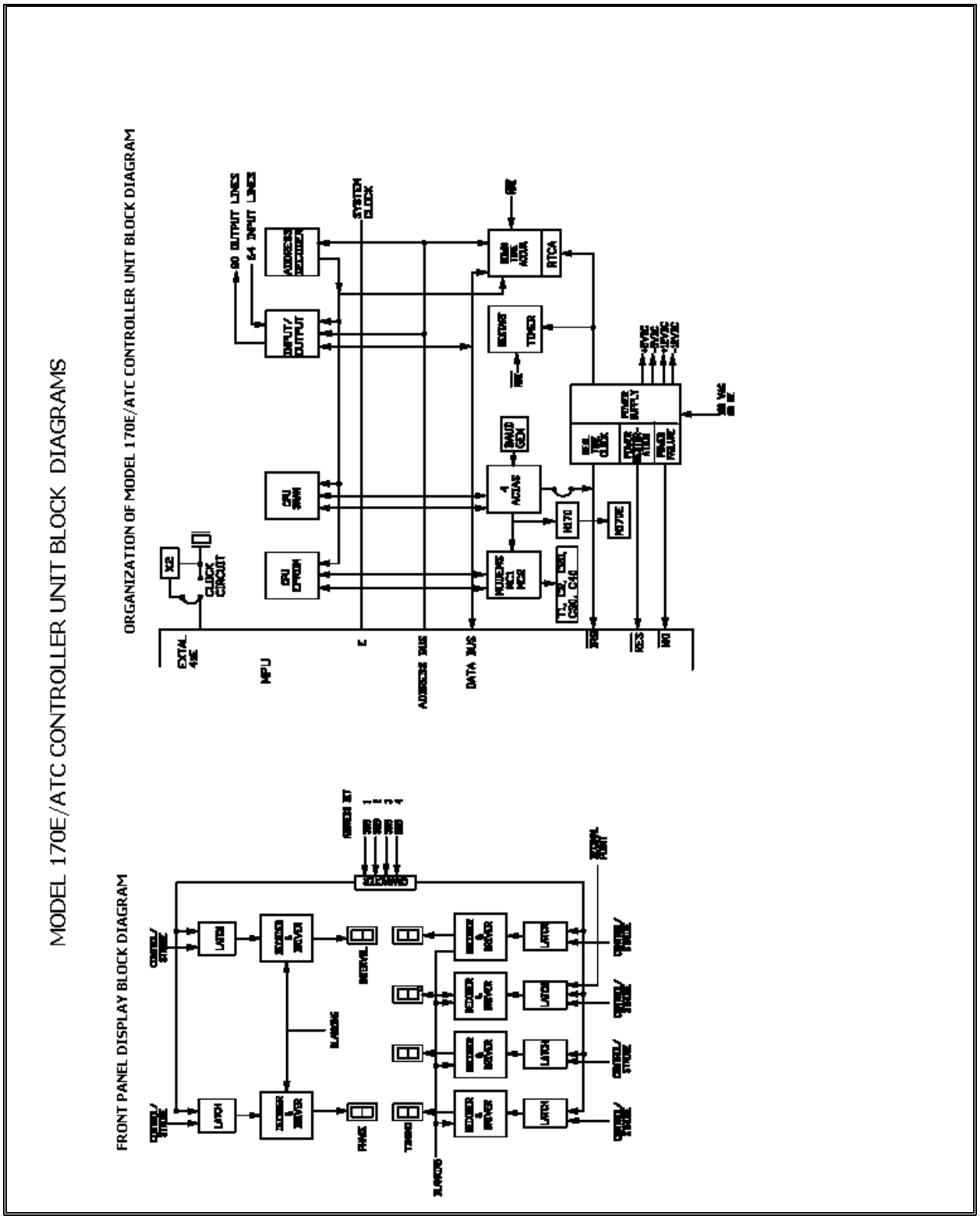


Figure 3-19: MODEL 170E-ATC CONTROLLER BLOCK DIAGRAMS

3.11.4 MODEL 170E-ATC TOP VIEW

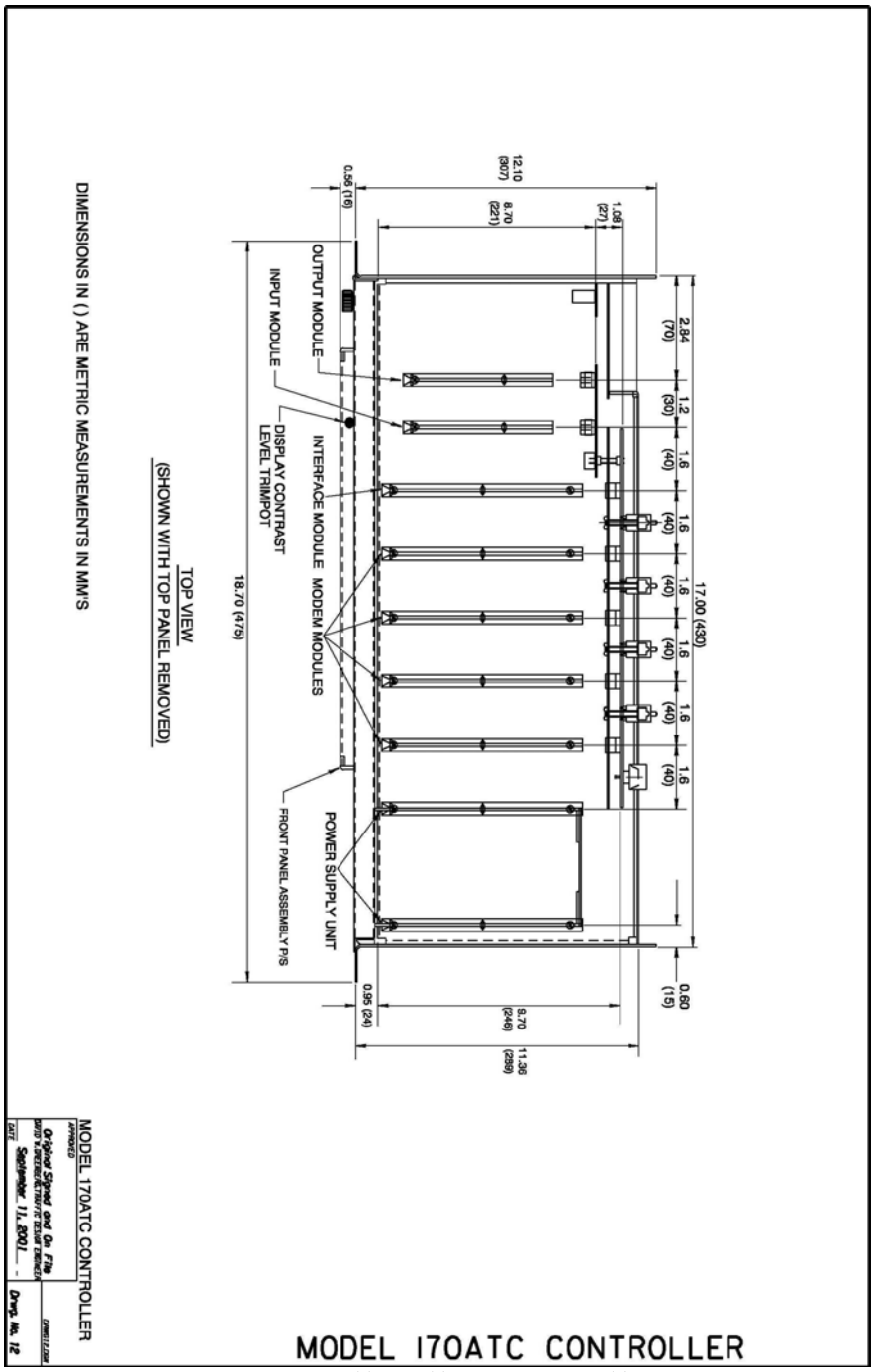


Figure 3-20: OREGON SSMSC DRAWING NO. 12, MODEL 170E-ATC CONTROLLER CHASSIS (TOP VIEW) Note: does not show the four DB9 connectors.

3.11.5 MODEL 170E-ATC FRONT VIEW

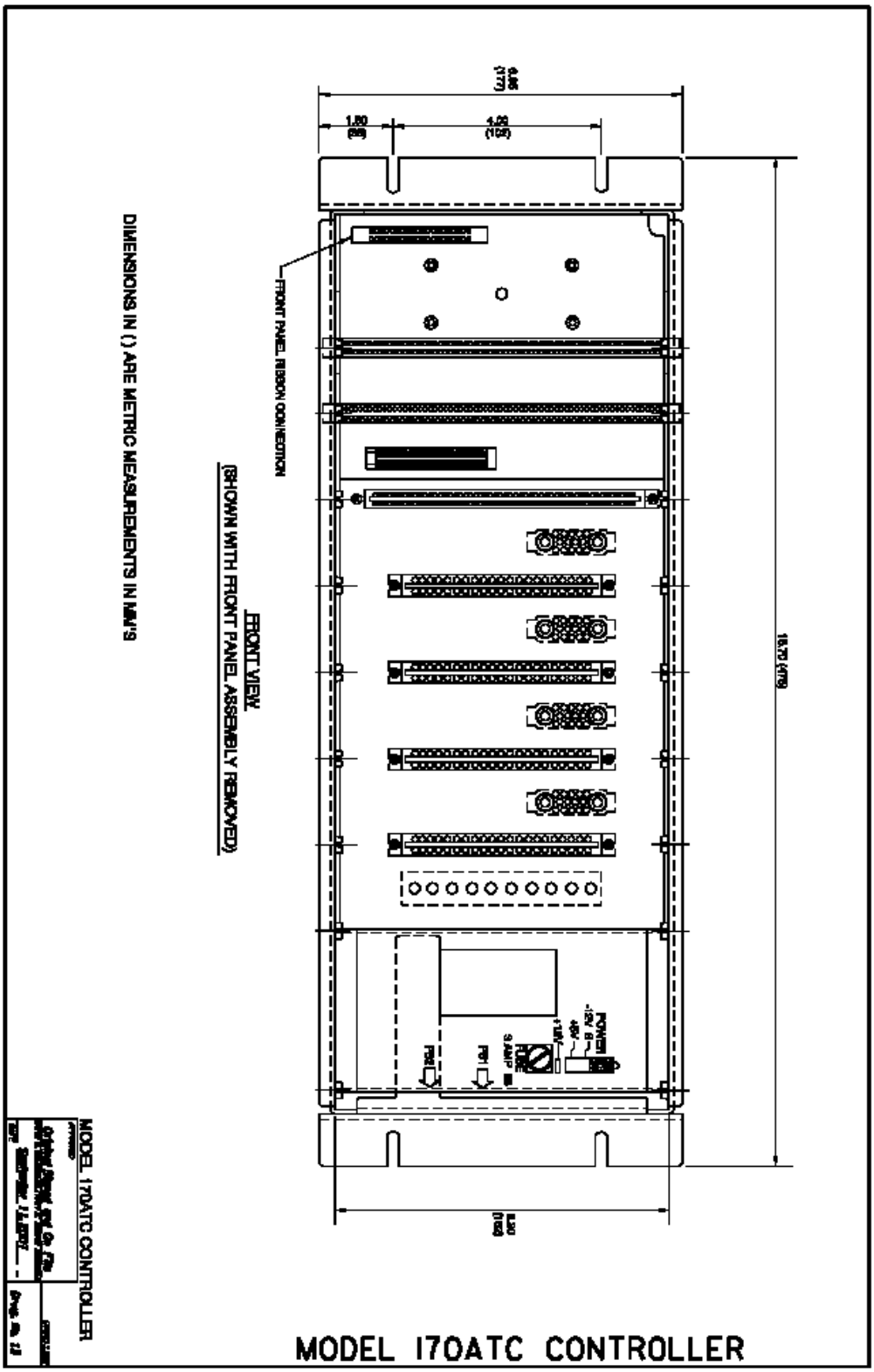


Figure 3-21 OREGON SSMSC DRAWING NO. 12, MODEL 170E-ATC CONTROLLER CHASSIS (FRONT VIEW) Note: does not show the four DB9 connectors.

3.11.6 MODEL 170E-ATC REAR VIEW

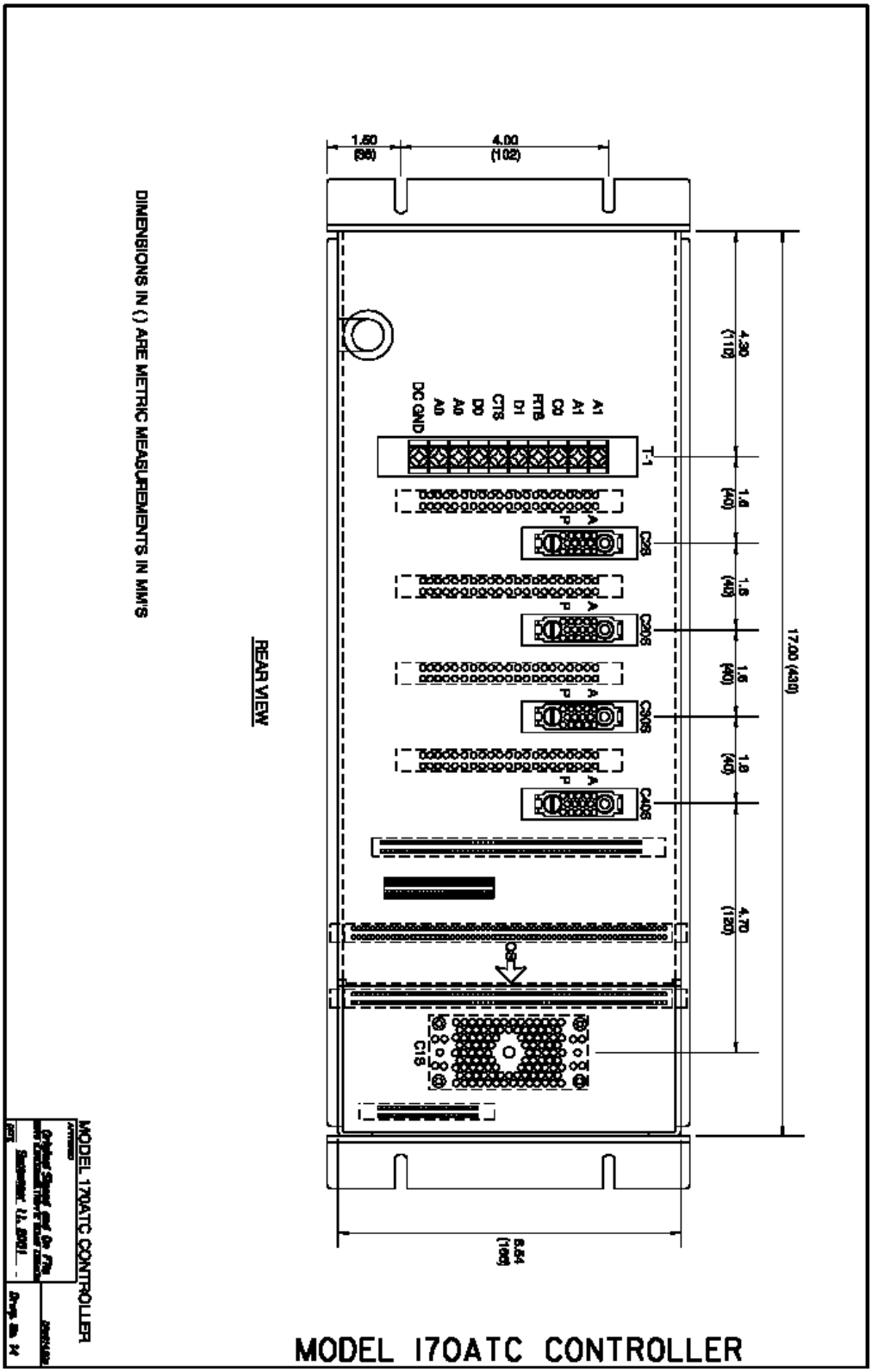


Figure 3-22: 170E-ATC CONTROLLER CHASSIS (REAR VIEW) *Note: does not show the four DB9 connectors.*

CHAPTER 4 MODEL 200 LOAD SWITCH and MODEL 204 FLASHER

Section 1 GENERAL

4.1.1 The module chassis shall provide rigid unit support for connector mounting PCBA support, module alignment and insertion/removal. It shall provide Triac heat sinking, and shall be made of metal meeting supportive and environmental requirements. Where electrical isolation protection is the only requirement, plastic insulation material may be used in lieu of metal.

4.1.2 Module control circuitry shall be readily accessible by the use of a screwdriver or wrench. Only one type of screw (slotted or Phillips) shall be used throughout.

4.1.3 Each module shall be so constructed that persons inserting or removing the module will not be exposed to any parts having live voltage. A handle shall be attached to the front of each module to facilitate the module insertion or removal from its mating connector.

4.1.4 The module shall be so constructed that its lower surface will be no more than 2.10 inches below the centerline of the connector and that no part will extend more than 0.90 inch to the left or 1.10 inches to the right of the centerline of the connector pin array.

4.1.5 Continuous edge guides shall be provided on the module.

4.1.6 The front panel of the module shall be provided with one indicator per switch. The indicators shall be vertically centered on the front panel with top and bottom indicators no more than one inch from the panel vertical center.

4.1.7 The front panel of the module shall be labeled with the manufacturer's name and the appropriate model number.

4.1.8 Each switch shall have the capability of switching any current from 0.05 to 10 amperes (AC) of tungsten lamp load or gas-tubing transformer load over a voltage range of 90 to 135 volts at 60 hertz and a temperature of 70 degrees C.

4.1.9 Each switch shall turn ON within ±5 degrees of the zero voltage point of the AC sinusoidal line, and shall turn OFF within ±5 degrees of the zero current point of the alternating current sinusoidal line. After power restoration, the zero voltage turn ON may be within ±10 degrees of the zero voltage point only during the first half cycle of line voltage during which an input signal is applied. Turn ON and OFF shall be within 8.33 msec following application or removal of the logic signal, respectively.

4.1.10 Each switch shall be designed for a minimum of 30 million operations while switching a tungsten filament load of 1,000 watts at 70 degrees Celsius.

4.1.11 Each switch shall have isolation between input DC control and AC to lights output circuit of at least 2,000VDC and 10,000 Megohms DC.

4.1.12 Each switch shall have 50 Megohms minimum DC resistance from the output to earth ground.

4.1.13 Each switch shall have a one-cycle surge rating of 175 amperes RMS and a one second surge rating of 40 amperes RMS.

4.1.14 Each switch shall be capable of withstanding a peak inverse voltage of 500 volts at 70 degrees C and no more than 20 mA leakage.

4.1.15 The connector plug contact tails shall be solder hook or eye styles only.

Section 2 MODEL 200 LOAD SWITCH

4.2.1 The Model 200 Solid State Load Switch shall be a modular plug-in device containing three solid-state switches to be used for opening and closing connections between the applied power and an external load.

4.2.2 A LOW state input (negative true logic) from the controller unit (saturated NPN transistor, 0 to +6VDC) shall cause the switch to be energized. A HIGH state input (cutoff NPN transistor, 16VDC or greater) shall cause the switch to de-energize. The state transition (conducting to nonconducting or vice versa) shall occur between six and 16VDC.

4.2.3 The incoming logic signal shall not sink more than 15 mA nor be subjected to more than 30VDC.

4.2.4 The module shall not draw more than 45 mA at +16VDC or greater from the cabinet power supply with all switches ON.

4.2.5 Each switch shall have an OFF state dv/dt rating of 100 volts per µsec or greater.

4.2.6 The indicators shall be labeled or color-coded from top to bottom "Red", "Yellow", and "Green". Each indicator shall indicate a controller unit output circuit.

4.2.7 The input circuit of each switch shall have reverse polarity protection up to 30VDC.

4.2.8 The resistance between the AC+ input terminal and the AC output terminal of each switch shall be 15,000 ohms minimum, when the switch is in the open position. The output current from the switch through the load when the load switch is in the OFF state shall not exceed 15 mA peak.

4.2.9 Each switch shall be isolated so that line transients or switch failure will not adversely affect the controller unit.

4.2.10 The Plug Connector shall be a BEAU P-5412-LAB or equal.

Section 3 MODEL 204 FLASHER

4.3.1 The Model 204 Flasher Unit shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. Its function shall be to alternately open and close connections between the applied power and an external Traffic Signal lamp load during intersection flashing operation.

4.3.2 The module shall generate its own internal DC power, from the AC line, for logic and control.

4.3.3 The module shall commence flashing operation when AC power is applied to the module.

4.3.4 The circuit shall provide 50 to 60 flashes per minute with a 50% duty cycle.

4.3.5 A surge arrestor shall be provided between AC+ (pin 11) and Flasher Out (pins 7 & 8). The surge arrestor shall be capable of reducing the effects of a transient voltage applied to the field signal circuits, and shall have the following ratings:

Recurrent peak voltage	212 Volts
Energy rating, maximum	50 Joules
Power dissipation, average	0.85 Watt
Peak current for pulses less than 6 µs	2000 Amperes
Standby current, less than	1 mA

4.3.6 3.3.6 Each switch shall have an OFF state dv/dt rating of 200 volts per µsec or greater.

4.3.7 The indicators shall indicate the output state of the switches.

4.3.8 The Plug Connector shall be a BEAU P-5406-LAB or equal.

4.3.9 Each circuit shall be designed to operate in an open circuit (without load) condition for a minimum of 10 years.

Section 4 CHAPTER DETAILS

4.4.1 MODEL 200 SWITCH PACK and 204 FLASHER UNITS

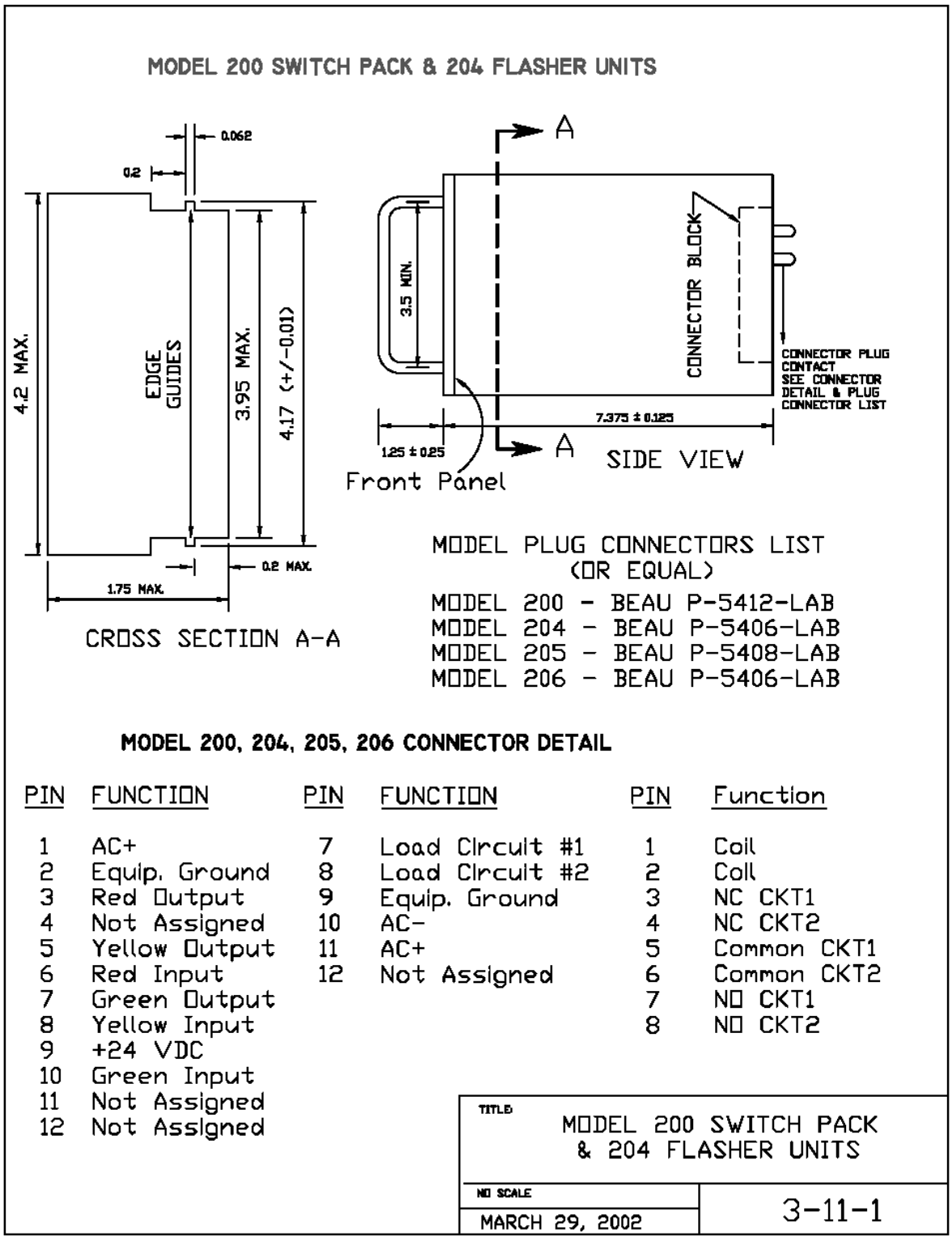


Figure 4-1: MODEL 200 SWITCH PACK AND 204 FLASHER UNITS

CHAPTER 5 MODEL 210E CONFLICT MONITOR UNIT

Section 1 SCOPE

5.1.1 This specification establishes minimum standards for Conflict Monitoring Devices designed for use with 170, 170E and 170E-ATC Controllers in Model 33x Traffic Signal Controller Cabinets supplied to the County of Los Angeles.

5.1.2 The scope of this specification encourages development of new designs and enhancements. New designs may be submitted for Acceptance Testing, to the County.

5.1.3 Reference is made to CHAPTER 1Section 1 above(Scope). The County remains the sole judge on the ability of each device to meet specifications.

Section 2 GENERAL

5.2.1 The Model 210E Monitor Unit is designed to monitor Green, Yellow, and Red AC circuits at the output terminals in Traffic Signal cabinets. In addition, the cabinet +24VDC supply, and the Model 170E controller Watchdog Timer outputs are also monitored. These signals are processed by the Monitor Unit circuitry, and if a failure is determined to have occurred, a relay output contact closure (FAILED state) places the cabinet and intersection in flashing operation

5.2.2 All monitored field output voltages shall be measured as true RMS (DC to 3 KHz) responsive to positive half-sine waves, negative half-sine waves as well as the full-sine waves.

5.2.3 Dimming algorithms (such as alternating or omitting a cycle) shall not compromise the monitor's ability to detect Fault conditions.

5.2.4 The Front Panel shall be removable without unsoldering connections.

5.2.5 FAILED STATE OUTPUT CIRCUITS

5.2.5.1 An electro-mechanical relay shall be used to provide an output circuit during a FAILED state. The relay contacts shall be normally closed (FAILED STATE). In a NON-FAILED state (relay coil energized), the contacts shall be open. The function of this output circuit is to energize the cabinet Mercury Contactor Coil and transfer field outputs from the Output File Load Switches to the Flasher Unit during a FAILED state.

5.2.5.2 The relay contacts shall be rated for a minimum of 3 amperes at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 msec or less.

5.2.5.3 A second output circuit (Stop Time input to the controller unit) shall be provided to sink a NPN Open Collector Transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50-mA load to less than 1.5 VDC in the active state. A blocking diode shall be provided on the transistor output to prevent it from sourcing power into the controller unit.

5.2.6 MONITOR UNIT RESET

5.2.6.1 An Internal Reset (front panel momentary pushbutton switch labeled "RESET") and External Test Reset input shall be provided to reset the Monitor to normal operation.

5.2.6.2 The Internal Reset switch shall be positioned so that it can be depressed while gripping the front panel handle.

5.2.6.3 The External Test Reset input line shall be optically isolated from the internal circuitry.

5.2.6.4 The monitor, once triggered by detection of a fault, shall remain in that state until a Reset Command is issued. Reset is issued only by the Internal Reset or by the External Test Reset input. A reset issuance by either source (Unit Reset) shall be trigged by only the leading edge (to prevent a constant reset from a switch failure or a constant external input).

5.2.7 Input impedance for all monitored AC inputs shall be 250K ohms (" 50K).

5.2.8 Both Monitor Unit and Programming Card Connectors shall be PCBA 28/56P Type.

5.2.9 Door Ajar Circuit: Pins 24 and 25 shall be connected together on the monitor PCBA at their connector fingers and be capable of carrying one ampere at +24 VDC.

5.2.10 All device sockets used in the design of the monitor shall be of a type deemed highly reliable and approved by the County.

5.2.11 Handle: The top of the handle cannot be less then 4 inches below the top edge of the monitor front panel. Any other handle placement must have prior approval from the county.

5.2.12 Fuse Holder: Fuse holders on the front panel must be the low profile type. Fuses shall be 1 ¼ by ¼ inches in size.

5.2.13 Battery: A battery may not be used.

5.2.14 EPROM Label: All UV erasable memory shall be protected from UV light. All microprocessors/microcontrollers and erasable memory with manufacture's firmware shall be labeled with their name and firmware revision.

5.2.15 Blank PCBA – One blank PCBA shall be supplied for each revision as a troubleshooting aid with every contract.

Section 3 FUNCTIONAL

5.3.1 **BASIC FEATURES:**

5.3.1.1 The Conflict Monitor Unit monitors the cabinet for unsafe operation. If an unsafe condition exists, the Monitor will enter into a Failed State.

5.3.1.2 The monitor shall be fully operational over a voltage range of 85VAC to 135VAC.

5.3.1.3 Voltages appearing at the channel inputs shall be analyzed and acted upon regardless of their phase relationship to the AC line voltage.

5.3.1.4 The Conflict Monitor shall sense and respond to Conflicts and 24VDC failures WHENEVER the AC line voltage is within the 85VAC to 135VAC operating range of the Monitor.

5.3.1.5 Means shall be provided to review status of the Green, Yellow and Red inputs of all channels, at the time the fault was latched. Power loss shall not affect the retention of this data.

5.3.1.6 Means shall be provided to selectively inhibit monitoring of Yellow inputs.

5.3.1.7 **ALL FAULTS SENSED BY THE MONITOR SHALL ONLY BE RESET BY THE FRONT PANEL RESET PUSHBUTTON OR EXTERNAL RESET INPUT!** In the event that the Monitor senses a fault, followed by a loss of operating voltage, the initial Failure Status shall be retained in memory and redisplayed after restoration of power.

5.3.1.8 It shall be possible to unplug the Monitor from the cabinet, and/or plug it in, without placing the cabinet into Flash operation (providing the cabinet door remains open).

5.3.1.9 It shall be possible to unplug the Red Monitoring Connector, P20, or plug it in, without placing the cabinet into Flash operation.

5.3.1.10 If a microprocessor is used in the Monitor design, its program shall be written so that:

5.3.1.10.1 Integrity tests shall be performed periodically on EACH memory cell of EACH memory device, relevant to each device type.

5.3.1.10.2 Hardware external to the microprocessor circuits shall be employed to constantly sense proper microprocessor operation.

5.3.1.10.3 If a fault is detected with the microprocessor, or with the integrity tests, the Monitor shall be triggered, and a front panel indicator shall latch ON to indicate an INTERNAL FAILURE.

5.3.2 EXTENDED FEATURES:

5.3.2.1 In addition to the features of the State 210 Monitor Unit, the Conflict Monitor Unit shall be designed to monitor multiple outputs, lack of outputs and duration of yellow interval. These comprise the Extended Features.

5.3.2.2 To utilize Extended Features, the Monitor requires a Red Enable Signal. Extended Features apply only to channels selected for Red Monitoring by turning the channel's DIP-switch ON.

5.3.2.3 The Conflict Monitor shall also detect when yellow time is less than an operator-set minimum, or if a sequence error (green-to-red transition with no yellow) occurs. (Yellow failure)

5.3.3 FRONT PANEL INDICATORS:

5.3.3.1 All indicator lights shall be water clear (not colored), not diffused lenses, Ultra-Bright, T-1 package LED's, Leadtech LT0373-41 (Red), LT0323-41-HE (Green), LT0333-41-UR (Yellow) or equivalent with a minimum luminous intensity of 100 mcd at 20 mA. Indicator lights shall be clearly visible in direct sunlight.

5.3.3.2 The AC POWER indicator shall be GREEN. Fault indicator lights shall be RED. Channel indicator lights shall be RED, unless there are three indicators per channel. In that case, each channel will have one red, one yellow, and one green indicator.

5.3.3.3 Indicator lights shall be arranged in a one vertical pattern with AC Power on top, Fault status lights as the upper indications, and the Channel lights as the lower indications.

5.3.3.4 Where there are three indicators per channel, the indicators shall form three columns, with the red to the left, yellow in the center and green to the right.

5.3.3.5 A Fault shall cause only the corresponding Fault indicator and appropriate channel indicators to display.

5.3.3.6 The indicators shall be labeled to provide the information described below:

5.3.3.6.1 AC POWER: Shall illuminate when the incoming AC Line Voltage exceeds 103 (±2) VAC, and shall FLASH at a ½ Hz rate if the line voltage drops below 103 (±2) VAC.

5.3.3.6.2 VDC FAILED: Shall illuminate when the Monitor has detected a 24 VDC failure.

5.3.3.6.3 CONFLICT: Shall illuminate when a conflicting signal condition has been detected. Active inputs shall be displayed on the channel indicators.

5.3.3.6.4 WDT ERROR: Shall illuminate when an error has been detected in the Controller watchdog output, and shall FLASH at a ½ Hz rate WHENEVER the Watchdog monitoring circuit is DISABLED.

5.3.3.6.5 DIODE CARD AJAR: Shall illuminate when the diode-programming card has been pulled out or is not properly seated in its slot.

5.3.3.6.6 MULTIPLE OUTPUT: Shall illuminate when the Monitor detects INPUT ON MORE THAN ONE of the inputs that comprise a monitored channel. The failing channel shall be displayed on the channel indicators.

5.3.3.6.7 LACK-OF-OUTPUT: Shall illuminate when the Monitor detects that there is NO INPUT on ANY of the inputs that comprise a monitored channel. The failing channel shall be displayed on the channel indicators. In addition, this indicator shall flash at a ½ Hz rate if the AC+ for Red Enable is not present.

5.3.3.6.8 YELLOW ERROR: Shall illuminate when the Monitor detects that a yellow did not follow a green, (green/red sequence error), or if yellow timing was less than a selected minimum. The failing channel shall be displayed on the channel indicators.

5.3.3.6.9 INTERNAL FAILURE: Shall illuminate to indicate a failure of the Monitor Microprocessor. (Required only if a Microprocessor is used).

5.3.3.6.10 When the Status and Failure indicator (s) are latched, due to a detected failure, only those indicators pertinent to the CAUSE of the failure shall be latched.

5.3.4 CARD EDGE CONNECTOR PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	Channel 2 Green	A	Channel 2 Yellow
2	Channel 13 Green	B	Channel 6 Green
3	Channel 6 Yellow	C	Channel 15 Green
4	Channel 4 Green	D	Channel 4 Yellow
5	Channel 14 Green	E	Channel 8 Green
6	Channel 8 Yellow	F	Channel 16 Green
7	Channel 5 Green	H	Channel 5 Yellow
8	Channel 13 Yellow	J	Channel 1 Green
9	Channel 1 Yellow	K	Channel 15 Yellow
10	Channel 7 Green	L	Channel 7 Yellow
11	Channel 14 Yellow	M	Channel 3 Green
12	Channel 3 Yellow	N	Channel 16 Yellow
13	Channel 9 Green	P	(Not assigned)
14	(Not assigned)	R	Channel 10 Green
15	Channel 11 Yellow	S	Channel 11 Green
16	Channel 9 Yellow	T	(Not assigned)
17	(Not assigned)	U	Channel 10 Yellow
--		--	
18	Channel 12 Yellow	V	Channel 12 Green
19	(Not assigned)	W	(Not assigned)
20	Chassis Ground	X	(Not assigned)
21	AC-	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	Tied to Pin 25	BB	Stop Time (Output)
25	Tied to Pin 24	CC	(Not assigned)
26	(Not assigned)	DD	(Not assigned)
27	(Not assigned)	EE	Output Switch, Side #2
28	Output Switch, Side #1	FF	AC+
-- Slotted for keying between Pins 17 and 18 (Pins U and V)			

Figure 5-1: CARD EDGE CONNECTOR PIN ASSIGNMENTS

5.3.5 **RED MONITORING CONNECTOR**

5.3.5.1 A connector (3M: 3428-5302, with two 3518 polarizing keys, or equivalent) shall be mounted on the Monitor front panel. Another connector of the same type, designated P20, is mounted near the rear of the cabinet output file. A ribbon cable 24 (±2) inches joins these connectors in length, provided with each unit. The connectors on the ends of the ribbon cable shall be of a closed type, to avoid electrical shock. The pin assignments of the P20 connector and terminal assembly shall be as shown below. Any P20 connector incorporating variations or additions to this specification shall be submitted to the County for approval prior to delivery of the sample unit.

5.3.5.2 P20 CONNECTOR PIN ASSIGNMENTS:

PIN	FUNCTION	TERMINAL BLOCK	PIN	FUNCTION	TERMINAL BLOCK
1	Channel 15 Red	15	11	Channel 9 Red	9
2	Channel 16 Red	16	12	Channel 8 Red	8
3	Channel 14 Red	14	13	Channel 7 Red	7
*4	Chassis Ground	17	14	Channel 6 Red	6
5	Channel 13 Red	13	15	Channel 5 Red	5
*6	Special Func.2	18	16	Channel 4 Red	4
7	Channel 12 Red	12	17	Channel 3 Red	3
*8	Special Func.1	19	18	Channel 2 Red	2
9	Channel 10 Red	10	19	Channel 1 Red	1
10	Channel 11 Red	11	20	Red Enable	20

Figure 5-2: P20 CONNECTOR PIN ASSIGNMENTS

5.3.5.3 Keying shall be between pins 3 & 5, and 17 & 19. (The odd numbered pins are on one side, and the even pins are on the other). The P20 connector and the CMU connector shall be keyed physically alike to prevent the Red Monitoring cable from being inserted into the P20 180 degrees out of alignment.

5.3.5.4 **RED ENABLE INPUT**

5.3.5.4.1 Pin 20 of the Red Monitoring Connector shall provide the Red Enable input to the monitor. When the Red Monitoring Connector is disconnected, or Red Enable is not present, the Monitor shall function as a standard Model 210 Monitor, checking for conflicting Greens and/or Yellows, controller Watchdog signal, and cabinet +24VDC power supply. When enabled, all Monitor functions shall become active, including the Lack-of-Output, Multiple Output, and Yellow Fail capabilities of the monitor.

5.3.5.5 **SPECIAL FUNCTION 1 AND 2 INPUTS**

5.3.5.5.1 Pin 6 and Pin 8 (Special Function 2 and 1) is for future use.

5.3.5.5.2 Means shall be provided to select either a PRESENCE of, or LACK of AC+ to enable these inputs.

5.3.6 **MONITORING OF CONFLICTING VOLTAGES**

5.3.6.1 Inputs to any channel, which are of sufficient level to exceed the set conflict threshold, shall be sensed as "ON" and shall illuminate their respective indicators.

5.3.6.1.1 The number of active channels shall in no way affect the conflict threshold or the level at which channels are sensed as "ON".

5.3.6.2 The following levels and times apply to full-wave, positive half-wave or negative half-wave inputs. The phase relationship of the input signals and the line voltage SHALL NOT affect the ability of the monitor to sense the defined input levels. For clarification of HALF-WAVE measurements, 15 Volts RMS is equivalent to a 21-Volt peak signal, and 25 Volts RMS is equivalent to a 35-Volt peak signal (half of a pure sine wave input only).

5.3.6.2.1 Sensing of conflicting voltages, at the field terminals, of 25 Volts RMS or greater for a duration of 450 msec or longer shall cause a FAILED state.

5.3.6.2.2 Sensing of conflicting voltages, at the field terminals, of 15 Volts RMS or less OR any voltage sensed ON having duration of 200 msec or less shall NOT cause a FAILED state.

5.3.6.2.3 Sensing of conflicting voltages, at the field terminals, of between 15 and 25 Volts RMS, OR any conflicting voltages sensed ON for duration's between 200 and 450 msec MAY or MAY NOT cause a FAILED state.

5.3.6.3 The watchdog, stop time, external reset, and 24V monitor input circuits shall be isolated from the conflict monitor internal power supply. Where the cabinet 24VDC-power supply is used to power these circuits, it shall be conditioned to provide proper sense circuit operation, even under low voltage or high ripple conditions.

5.3.7 **CONFLICT PROGRAMMING CARD**

5.3.7.1 A plug-in PCBA Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match one through 16 channels of possible conflict. The programming card shall be logically arranged and labeled for easy identification of the diodes by channel. With diodes in place, all output channels being monitored shall be in conflict. When the diode has been removed, the channels shall be interpreted as non-conflicting.

5.3.7.2 The programming card shall be 6 inches in depth and 5.15 to 5.30 inches in height, and shall intermate with a 28/56 pin double-sided connector having bifurcated contacts on 0.156-inch centers. The printed circuit board shall bisect its edge board fingers at their centers to within ±0.016 inches. The center of the edge board fingers shall be 2.6375 inches from either edge of the board. The programming card, when installed, shall be provided with card ejectors for removal from the front panel. It shall be flush with the front panel and slide smoothly on its track while being inserted into or removed from the monitor module.

5.3.7.3 PROGRAMMING CARD CONNECTOR PIN ASSIGNMENTS:

Pin	FUNCTION (circuit side)	Pin	FUNCTION (component side)
1	Channel 2 Green	A	Channel 1 Green
2	Channel 3 Green	B	Channel 2 Green
3	Channel 4 Green	C	Channel 3 Green
4	Channel 5 Green	D	Channel 4 Green
5	Channel 6 Green	E	Channel 5 Green
6	Channel 7 Green	F	Channel 6 Green
7	Channel 8 Green	H	Channel 7 Green
8	Channel 9 Green	J	Channel 8 Green
9	Channel 10 Green	K	Channel 9 Green
10	Channel 11 Green	L	Channel 10 Green
11	Channel 12 Green	M	Channel 11 Green
12	Channel 13 Green	N	Channel 12 Green
13	Channel 14 Green	P	Channel 13 Green
14	Channel 15 Green	R	Channel 14 Green
15	Channel 16 Green	S	Channel 15 Green
16	DC GROUND	T	CONFLICT
17	Channel 1 Yellow	U	Channel 9 Yellow
18	Channel 2 Yellow	V	Channel 10 Yellow
19	Channel 3 Yellow	W	Channel 11 Yellow
20	Channel 4 Yellow	X	Channel 12 Yellow
21	Channel 5 Yellow	Y	Channel 13 Yellow
22	Channel 6 Yellow	Z	Channel 14 Yellow
23	Channel 7 Yellow	AA	Channel 15 Yellow
24	Channel 8 Yellow	BB	Channel 16 Yellow
--		--	
25	not assigned	CC	Not assigned
26	not assigned	DD	Not assigned
27	Not assigned	EE	Not assigned
28	Yellow Inhibit Common	FF	Not assigned

Figure 5-3: PROGRAMMING CARD CONNECTOR PIN ASSIGNMENTS

5.3.7.4 Pads for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin and the yellow inhibit common shall disable sensing the said channel yellow.

5.3.7.5 The programming card shall inter mate with a PCBA 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provide a mechanically sound card and connector support including

continuous card guides. When the programming card is resident in the unit, the card's front end shall be flush with the unit's front panel.

5.3.7.6 Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.

5.3.8 WATCHDOG TIMER:

5.3.8.1 DEFINITION OF WATCHDOG OPERATION:

5.3.8.1.1 When **Red Enable** Input is ON: Monitoring of the Watchdog SHALL NOT BE INHIBITED BY ANY THRESHOLD.

5.3.8.1.2 Otherwise, monitoring of the watchdog shall function as specified below:

5.3.8.1.2.1 The Watchdog Circuitry shall sense the incoming AC line voltage, and when the voltage DROPS BELOW 98 (±2) VAC for 50 (±17) msec, monitoring of the controller Watchdog shall be INHIBITED. Loss of AC line voltage for less than 50 msec shall be ignored.

5.3.8.1.2.2 When the incoming AC line voltage RISES ABOVE 103□(±2) VAC for 50 (±17) msec, monitoring of the controller Watchdog shall RESUME.

5.3.8.1.2.3 A minimum hysteresis of 5 volts shall be maintained between the INHIBIT voltage level (as the AC line voltage is reduced) and the ENABLE voltage level (as the AC line voltage is raised).

5.3.8.2 A WATCHDOG INHIBIT SWITCH SHALL NOT BE INSTALLED *(NOTE: This switch was only needed for cabinet testing. It is no longer needed*). An absence of valid Watchdog signal input for a period of 1.0 second (±100msec) shall cause a FAILED state EXCEPT:

5.3.8.2.1 If the Watchdog Monitoring function is disabled due to a low voltage condition. (See Section 4.4.5: "Brownout/Power Fail Recovery")

Section 4 ELECTRICAL

5.4.1 The monitor shall be operational over a voltage range of 85 VAC to 135 VAC.

5.4.2 Chassis Ground and AC- shall be isolated from one another.

5.4.3 **MONITORED AC INPUTS**

5.4.3.1.1 The following levels and times refer to full wave, positive half-wave and negative half-wave inputs: (See SECTION 4.3.5.2 for clarification of half-wave measurements)

5.4.3.1.2 GREEN AND YELLOW INPUTS -

Any inputs < 15 VRMS shall be considered OFF

Any inputs > 25 VRMS shall be considered ON

5.4.3.1.3 TIMING OF CONFLICTING INPUTS -

Inputs on < 200 msec shall be considered NO FAULT.

Inputs on > 450 msec shall be considered a FAULT.

5.4.3.1.4 YELLOW TIMING:

Measured Yellow time less than an operator-set value, OR a green-to-red transition with no yellow, shall be considered a FAULT,

EXCEPT in the event of a Brownout condition, as specified in Section 4.4.5: Brownout/Power Fail Recovery.

5.4.3.1.5 RED INPUTS

Any inputs < 50 VRMS shall be considered OFF□Any inputs > 70 VRMS shall be considered ON

5.4.3.1.6 LACK-OF-OUTPUT TIMING

Lack of input for < 700 msec shall be considered NO FAULT.

Lack of input for > 900 msec shall be considered a FAULT.

5.4.3.1.7 MULTIPLE OUTPUT TIMING

Multiple inputs for < 700 msec shall be considered NO FAULT.

Multiple inputs for > 900 msec shall be considered a FAULT.

5.4.3.1.8 RED ENABLE INPUT

Input < 50 VRMS shall be considered OFF

Input > 70 VRMS shall be considered ON

5.4.3.1.9 SPECIAL FUNCTION 1 AND 2 INPUTS

Input < 50 VRMS shall be considered a LOW *

Input > 70 VRMS shall be considered a HIGH *

* HIGH or LOW enable shall be Operator Selectable□

5.4.4 MONITORED DC INPUTS

5.4.4.1 +24 VDC INPUT

Input < 18VDC shall be considered a FAULT

Input > 22VDC shall be considered NO FAULT

5.4.4.1.1 +24 VDC TIMING

Input < 18 VDC for < 200 msec shall be considered NO FAULT.

Input < 18 VDC for > 500 msec shall be considered a FAULT.

5.4.4.1.2 WATCHDOG MONITOR INPUT

Input < 4 VDC shall be considered a LOW

Input > 12 VDC (or OPEN) shall be considered a HIGH

5.4.4.1.3 WATCHDOG ERROR TIMING

Lack of valid input signal changes for < 900 msec = NO FAULT

Lack of valid input signal changes for > 1100 msec = a FAULT

5.4.5 BROWNOUT/POWER FAIL RECOVERY

5.4.5.1 If the RED ENABLE Input is ON, the Conflict Monitor shall determine that a Brownout has occurred if:

AC line voltage dropped below 98 (±2) VAC, AND Lack-of-Output was recorded on ALL channels enabled for Lack-of-Output monitoring.

5.4.5.1.1 If BOTH of the above conditions are met, the Monitor WILL NOT LATCH a Lack-of-Output error, Watchdog error, or Yellow Fail error and WILL NOT place the cabinet in FLASH operation.

5.4.5.1.2 Recovery to full normal monitoring of Lack-of-Output, Controller Watchdog, and Yellow Fail shall resume when:

5.4.5.1.3 ANY GREEN or YELLOW or RED is sensed on ANY channel enabled for LACK-OF-OUTPUT monitoring, OR

5.4.5.1.4 When a change of state in the Controller Watchdog is sensed, OR when the incoming AC line voltage reaches 103 (±) VAC

5.4.5.2 If the RED ENABLE Input is NOT ON or there are NO CHANNELS ENABLED FOR LACK-OF-OUTPUT sensing, the Conflict Monitor shall determine that a Brownout has occurred if the incoming AC line voltage DROPS BELOW 98 (±2) VAC for 50 (±17) msec or more. Loss of AC line voltage for less than 50 msec shall be ignored.

5.4.5.3 Monitoring of the Watchdog shall be inhibited when the incoming AC line voltage DROPS BELOW 98 (±2) VAC for 50 (±17) msec. Under these conditions, the Monitor shall NOT place the intersection into flashing operation.

5.4.5.4 Recovery to normal Watchdog monitoring operation shall occur when the incoming AC line voltage RISES ABOVE 103 (±2) VAC for 50 (±17) msec, providing NO OTHER Failures have been recorded.

Section 5 OPTIONAL DESIGN

5.5.1 **COUNTY APPROVAL:** Conflict Monitors using this design, including the Software support package, must be submitted as a Sample Unit and approved by the County prior to shipment.

5.5.2 Lack-of-Output, Multiple Output, and Yellow Fail functions shall be assignable to any channel in any combination.

5.5.3 Means shall be provided to off-load to an external device ALL Monitor parameter and permitted phase ("diode cut-out") data, checksum, and date programmed, via a RS-232C serial port mounted on the front panel of the unit. If the parameters of the port are not selectable, the format shall be; 1200 baud, 1 start bit, 1 stop bit, 7 data bits, and even parity. The connector on the monitor shall be a DB9S, wired as IBM AT DTE equipment.

5.5.4 The Supplier shall provide a Software Package capable of running on IBM compatible computers. Support documentation and manuals shall be included, along with the right to copy the software for operation on several County computers. Features of the Programming Software shall include, but not be limited to the following:

5.5.4.1 DEFAULT PROGRAM MODULE

5.5.4.1.1 A program module shall be provided to create and edit a minimum of four (4) tables containing the following parameters:

Conflict Time
Conflict Threshold
Lack-of-Output Time
Watchdog error Time
24 VDC Fail Time

5.5.4.1.2 Access to this default program module shall be restricted with a security code containing a minimum of four characters. Means shall be provided to change the security code as necessary.

5.5.4.2 MAIN PROGRAM

5.5.4.2.1 A Menu-driven main program shall be provided, with on-line "help" to guide the operator through all necessary programming parameter selections. The operator shall be prompted to select a table of parameters from those configured and available in the Default Program Module, with table 1 (L.A. County parameters) as the default choice.

5.5.4.2.2 Choosing another parameter table from those that are enabled shall be allowed, but the operator shall be prompted with a message indicating that the choice will result in non: County standard operation, and ask for confirmation.

5.5.4.2.3 Full edit capabilities shall be provided for all other programming functions. Data pertaining to intersection identification (four digits, minimum) and the date shall be entered by the operator, and form part of the data file. Upon completion of the parameter selections, a review feature will show which parameters have been selected. A checksum of all parameter data EXCEPT the date shall be displayed.

5.5.4.2.4 A Print feature shall be provided to produce a "diode card" showing which "diodes" have been cut, which "yellow inhibit jumpers" have been programmed, and a listing of the other parameter information, including the intersection I.D, checksum, and date.

5.5.4.2.5 The data, including the date and checksum, shall then be saved to disk in either INTEL Hex or Motorola format, utilizing the intersection identification as part of the file name.

5.5.4.2.6 A feature shall be provided to load an intersection parameter data file from a disk for observation or editing. This feature shall also utilize a user-friendly menu format, and provide review or printout of historical data by intersection.

5.5.4.2.7 A feature shall be provided to upload all parameter data from an operating monitor, without interruption of monitoring capability. The uploaded file would then be displayed and compared to the disk file, with

options to date and time stamp the uploaded file for historical data storage, and print out the data as described above.

Section 6 ADDITIONAL FEATURES

5.6.1 ADDITIONAL FEATURES The following features are NOT requirements of this specification. They are included for information only, and remain subject to COUNTY approval.

5.6.1.1 RIPPLE DETECTION This feature would monitor the 24 VDC cabinet power supply for ripple in excess of 5 volts Peak, and FLASH the 24 VDC FAIL front panel indicator, but WOULD NOT place the cabinet in flashing operation.

5.6.1.2 CURRENT MONITORING This feature would enhance, but not replace, the Lack-of-Output and Multiple Output features. By sensing and "remembering" the AC currents to the field, percentage variation parameters could be programmed to allow the Monitor to detect field problems due to lamp burnout or partial shorts to ground. Compensation for current variations due to normal fluctuation of AC line voltage should be incorporated into this design.

Section 7 CHAPTER DETAILS

5.7.1 MODEL 210 MONITOR UNIT

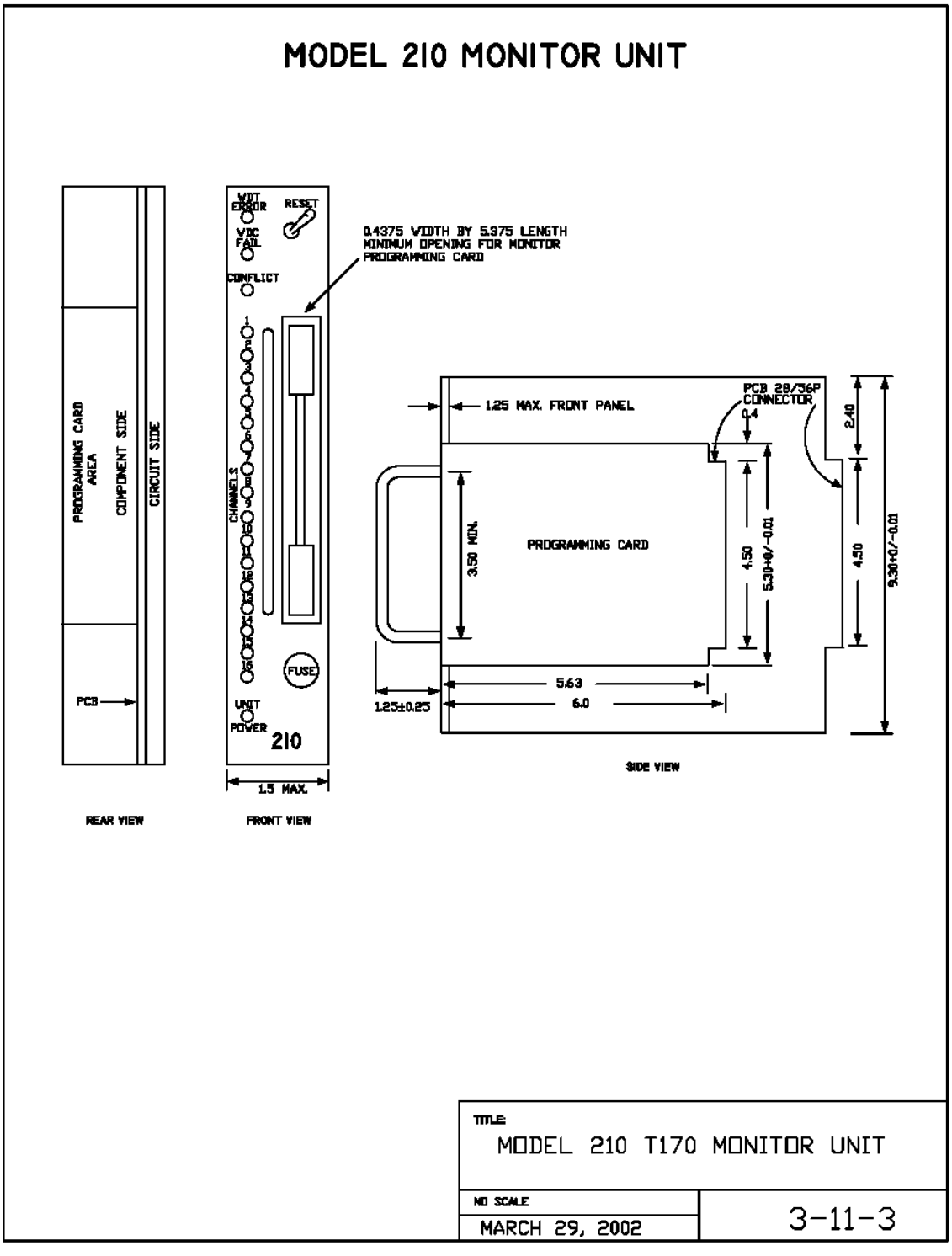


Figure 5-4: TEES DRAWING 3-11-3, MODEL 210 MONITOR UNIT

5.7.2 MODEL 210 MONITOR UNIT and PROGRAMMING CARD WIRING ASSIGNMENTS

MODEL 210 MONITOR UNIT CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION	Pin	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #8 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #6 Yellow	F	Channel #15 Green
7	Channel #5 Green	H	Channel #5 Green
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 Green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC− *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25 Tied Together)	BB	Step Time
25		CC	NA
26	NA	DD	NA
27	NA	EE	Output SW. Side #2
28	Output SW. Side #1	FF	AC+

MODEL 210 PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION (Circuit Side)	Pin	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #15 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW. Side #2
28	Output SW. Side #1	FF	AC+

TITLE: MODEL 210 MONITOR UNIT & PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS	
NO SCALE	3−11−4
MARCH 29, 2002	

Figure 5-5: MODEL 210 MONITOR UNIT and PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

5.7.3 Programming Card Connector Wiring Assignments

MODEL 210 MONITOR UNIT CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION	Pin	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #6 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #8 Yellow	F	Channel #16 Green
7	Channel #5 Green	H	Channel #5 Green
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 Green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC− *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25	BB	Stop Time
25	Tied Together)	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

MODEL 210 PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION (Circuit Side)	Pin	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #15 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

TITLE: MODEL 210 MONITOR UNIT & PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

NO SCALE

TEES, NOV 19, 1999 | 3−11−4

Figure 5-6: Programming Card Connector Wiring Assignments

CHAPTER 6 DETECTOR SENSOR UNITS, ELEMENTS AND ISOLATORS

Section 1 GENERAL

6.1.1 **MECHANICAL**

6.1.1.1 The County reserves the right to reject any design incompatible with the County's needs

6.1.1.2 All sensor units and isolators shall be solid-state units that inter-mate with, and be compatible with, the standard Input Files in Models 332, 336, and 337 Traffic Signal Control Cabinets.

6.1.1.3 All sensor units and isolators shall be mounted on an edge-connected, printed circuit board. After all components have been mounted, each PCBA shall be treated with a clear, moisture-proof coating to provide environmental protection.

6.1.1.4 The numbered and lettered sides of the PCBA connector shall be commonly assigned.

6.1.1.5 The sensor unit or isolator front panel shall be provided with a hand pull to facilitate insertion and removal from the Input File.

6.1.1.6 Each sensor unit or isolator channel shall have a front panel mounted red 'water-clear' LED indicator to provide visual indication of the detection of an incoming signal. The indicator shall be on the output to the controller side of the logic circuit. The horizontal cone of visibility of the indicator for Models 222, 228, 232, 242, and 252 units shall be a minimum of ±15 degrees.

6.1.1.7 Generally, all switches should be accessible from the front panel.

6.1.2 **OPERATION**

6.1.2.1 Each sensor unit or isolator channel shall be operationally independent.

6.1.2.2 A switch or switch position shall be provided to call the output of each isolator channel on an individual basis, or to individually disable the channels of sensor units.

6.1.2.3 A valid channel input shall cause a channel ground true output of a minimum 125 msec duration.

6.1.2.4 The sensor unit or sensing element shall operate and interface reliably with an associated County approved Sensing Unit or Element.

6.1.2.5 The output transistor shall switch from the OFF state to the ON state in a period equal to or less than 20 µsec. The transistor shall switch from the ON state to the OFF state in a period equal to or less than 20 µsec.

6.1.2.6 Each channel of any detector sensor unit shall be capable of detecting the presence or passage of ALL type of California licensed vehicles when connected to appropriate sensing apparatus, then producing an output signal as described.

6.1.2.7 A malfunction of a vehicle sensor unit, its sensing element, or the lead-in cable, shall cause the sensor channel to output a constant signal, regardless of mode selected.

6.1.3 **ELECTRICAL**

6.1.3.1 The front panel and hand pull of all sensor units and isolators shall be connected to the chassis ground of the module.

6.1.3.2 Each sensor unit or AC isolator channel shall draw no more than 100 mA from the +24 VDC cabinet power supply, shall be insensitive to 700 millivolts RMS ripple on the incoming +24 VDC line, and operate normally within the specifications of the +24V power supply.

6.1.3.3 Each sensor unit or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs.

6.1.3.4 LIGHTNING PROTECTION

6.1.3.4.1 Lightning Protection shall be installed within the sensor unit or isolator unit.

6.1.3.4.2 The power line surge protection (including the Cabinet protection and that internal to the equipment) shall enable the equipment under test to withstand (nondestructive) and continue to operate normally following exposure to test signals (applied at the Cabinet Service Block). The test signals shall comply with ANSI/IEEE C62.41 (100kHz. Ring Wave, and the EFT Burst) at voltages and currents specified at "Location Category A1" (i.e. up to 2.0 kV, 0.07 kA for the 100kHz Ring Wave) and at up to "Test Severity" level I (i.e. up to 1.0 kV open-circuit) for the EFT Burst.

6.1.3.4.3 The EFT Burst test signal will be applied for 10 minutes. The Ring Wave and Combination Wave will each be applied at a rate of once every 10 seconds for a maximum for 50 occurrences per test.

6.1.3.4.4 The unit under test will be operated at 20 degrees (+ or - 5) Celsius and at 120 (+ or - 12) VAC.

6.1.3.4.5 Other types of plug-in units not described in this document must be submitted to the County for approval prior to being supplied for any project calling for County equipment specifications.

Section 2 MODEL 222 LOOP DETECTORS

6.2.1 **GENERAL**

6.2.1.1 The sensor unit channel shall produce an output signal when a vehicle passes over or remains over wire loops embedded in the roadway. The method of detection shall be based upon a design that renders an output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% (minimum) decrease in inductance of the circuit measured at the input terminals of the sensor unit. The detector zone shall include those created by all configurations listed in paragraph 5.2.2.4.2

6.2.2 **FUNCTIONAL REQUIREMENTS**

6.2.2.1 OPERATION

6.2.2.1.1 Detector units shall comply with all performance requirements of this specification when connected to an inductance (loop plus lead-in) of from 20 to 2000 μH with a Q-parameter as low as five at the detector operating frequency.

6.2.2.1.2 Selection of frequency, sensitivity, and mode shall be completely independent for each detector channel.

6.2.2.1.3 Loop inputs to each channel shall be transformer isolated.

6.2.2.2 TUNING

6.2.2.2.1 Tuning for each detector channel shall be automatic, and designed so that drift, which may occur due to the environment and/or applied power, shall not cause an actuation.

6.2.2.2.2 Each individual channel shall have a minimum of three switch selectable operating frequencies.

6.2.2.3 MODE SELECTION: Each detector channel shall have two switch selectable modes of operation Pulse, and Presence.

6.2.2.3.1 PULSE MODE

6.2.2.3.1.1 In the pulse mode, each new vehicle presence within the zone of detection shall initiate one detector channel output pulse of 125-(±25) milliseconds duration.

6.2.2.3.1.2 Should a vehicle remain in a portion of the zone of detection for a period in excess of 2 seconds, the detector channel shall automatically "tune out" the presence of the said vehicle. The recovery time between the first vehicle pulse and channel capability to detect another vehicle entering the same zone of detection shall be 3 seconds maximum.

6.2.2.3.2 PRESENCE MODE

6.2.2.3.2.1 In the presence mode, the detector channel shall recover to normal sensitivity within one second after termination of vehicle presence in the zone of detection, regardless of the duration of the presence.

6.2.2.3.2.2 With the sensitivity setting at its HIGHEST level, a vehicle that is within the zone of detection shall be detected for a minimum of three minutes when the inductance change is 0.02 percent, and a minimum of ten minutes when the vehicle causes a 0.06 percent inductance change.

6.2.2.3.2.3 With the sensitivity setting at its LOWEST level, a vehicle causing a one- percent or greater change in loop inductance shall be detected for a minimum of four minutes.

6.2.2.4 SENSITIVITY

6.2.2.4.1 Each detector channel shall be equipped with at least three front panel selectable sensitivity settings as follows:

LOW -- .32%
MED -- .08%
HIGH - .02%

6.2.2.4.2 Each detector channel shall respond to an inductance change of 0.02 percent when connected to the following three-turn loop configurations:

(1) Single 6' by 6' loop with a 250-foot lead-in cable.

(2) Single 6' by 6' loop with a 1000-foot lead-in cable.

(3). Four 6' by 6' loops connected in series/parallel with a 250 foot lead-in cable

(4) Four 6' by 6' loops connected in series with a 1000 foot lead-in cable.

6.2.2.4.3 Each detector channel, when in PRESENCE mode and the LOWEST sensitivity option is selected, shall respond to a nominal loop inductance change between 0.15 percent and 0.4 percent while connected to the above loop configurations. This setting shall NOT respond to an inductance change of less than 0.1 percent.

6.2.2.4.4 The detector channel shall NOT detect vehicles, moving or stopped, at distances of 3 feet or more from the perimeter of any of the loop configurations listed above.

6.2.2.4.5 No sensitivity settings shall differ more than ±40 percent from the nominal value chosen.

6.2.2.5 RESPONSE TIMING

6.2.2.5.1 Response time of the detector channel, when PRESENCE mode and LOWEST sensitivity are selected, shall be less than 20 msec. That is, for any negative inductive change that exceeds its sensitivity threshold, the channel shall output a ground true logic level within 20 msec.

6.2.2.5.2 When the change is removed, the output shall become an open circuit within 20 msec, subject to minimum output duration requirements.

6.2.2.5.3 The response time of the detector channel for the HIGHEST sensitivity setting shall be less than 250 milliseconds for a 1.0- percent inductance change.

6.2.3 **ELECTRICAL REQUIREMENTS**

6.2.3.1 APPLICATION OF POWER

6.2.3.1.1 The detector channels shall begin normal operation within 2 seconds, and be fully operational within 30 seconds after the application of power or the reset signal.

6.2.3.2 INTERFERENCE

6.2.3.2.1 The separate channels contained within a given unit shall include means to prevent cross talk with one another.

6.2.3.2.2 Each unit shall include means to prevent cross talk with other modules. If the prevention means is manual, the control for it shall be located on the front panel of the unit. No additional external wiring shall be required to implement the prevention means.

6.2.3.3 TRACKING RATE

6.2.3.3.1 The detector shall be capable of compensating or tracking for an environmental change up to 0.001 percent change in inductance per second.

6.2.3.4 TRACKING RANGE

6.2.3.4.1 The sensor unit shall be capable of normal operation, as the input inductance is changed ±5.0percentage from the quiescent tuning point regardless of internal circuit drift.

6.2.3.4.2 The sensor unit shall be capable of normal operation, as the input resistance is changed ±5.0percentage from the quiescent tuning point regardless of internal circuit drift.

6.2.3.5 TEMPERATURE CHANGE

6.2.3.5.1 The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance resulting from environmental changes where the rate of temperature change does not exceed 1 degree Celsius per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18 degrees Celsius between the inside and outside air shall not affect the proper operation of the sensor unit.

6.2.3.6 RESET: The detector unit shall respond to a ground reset signal of 15 µsec or longer and begin normal operation within 2 seconds after the reset command.

6.2.3.7 MODEL 222 LOOP DETECTOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS (C)=COLLECTOR (E)=EMITTER

PIN	FUNCTION	PIN	FUNCTION
A	DC Ground	N	Not connected
B	+24 VDC	P	Not connected
---	(keyed)		
C	Detector Reset	R	Not connected
D	Loop #1 Input	S	Not connected
E	Loop #1 Input	T	Not connected
F	Controller Output #1 (C)	U	Not connected
H	Controller Output #1 (E)	V	Not connected
J	Loop #2 Input	W	Controller Output #2 (C)
K	Loop #2 Input	X	Controller Output #2 (E)
L	Equipment Ground	Y	Not connected
M	Not connected	Z	Not connected
---	(keyed)		

Figure 6-1: Model 222 Loop Detector Board Edge Connector Pin Assignments

Section 3 MODEL 228 MAGNETOMETER and MODEL 227 SENSING ELEMENT

6.3.1 **GENERAL**

6.3.1.1 The method of detection shall be based upon sensing a change in the vertical component of the earth's magnetic field caused by the passage or presence of a vehicle over the detector-sensing element.

6.3.1.2 Design of the detector sensor unit shall be such that an open circuit or short circuit in the primary or the secondary windings of the sensing element shall cause a constant channel output signal regardless of selected operating mode.

6.3.1.3 A minimum of two modes of operation shall be available as follows:

6.3.1.3.1 PULSE MODE: The pulse mode of operation shall provide one output closure of 150-(±25) msec duration for any vehicle entering the area of detection.

6.3.1.3.2 PRESENCE MODE: The presence mode of operation shall signal continually the presence of a vehicle until the vehicle leaves the area of detection.

6.3.2 **FUNCTIONAL REQUIREMENTS, MODEL 228:**

6.3.2.1 Each sensor unit shall house two complete, fully independent detection channels. Each channel shall operate with an effective load of up to six sensing elements connected to it.

6.3.2.2 Each channel shall detect vehicles traveling at any speed from 0 to 80 miles per hour. (See 5.1.2.6)

6.3.2.3 Parked or stalled vehicles over probes of one channel shall have no effect on the operation of any other channel.

6.3.2.4 Damage to sensing elements or cables of one channel shall not affect operation of any other channel.

6.3.2.5 The detector shall operate at any distance up to 3000 feet between the sensor unit and the sensing elements.

6.3.2.6 Following a power interruption, the sensor unit shall return to normal operation within one minute.

6.3.2.7 The front panel of the sensor unit shall contain:

6.3.2.7.1 An indicator for each channel to indicate detection of a vehicle,

6.3.2.7.2 A switch for selecting the mode of operation,

6.3.2.7.3 Calibration/tuning controls for each detector channel, if not self-tuning.

6.3.2.8 All switches and controls shall be clearly and permanently identified and shall be operable without the use of tools or external meters.

6.3.3 **CONNECTOR REQUIREMENTS**

6.3.3.1 MODEL 228 DUAL-SLOT MAGNETOMETER BOARD EDGE CONNECTOR PIN ASSIGNMENTS (C)=Collector (E)=Emitter

PIN	FUNCTION	PIN	FUNCTION
A	DC Ground	N	AC+
B	+24 VDC	P	Sense Element #2 Input
---	(keyed)		
C	Detector Reset	R	Sense Element #2 Input
D	Sensing Element #1 Input	S	Controller Output #2 (C)
E	Sensing Element #1 Input	T	Controller Output #2 (E)
F	Controller Output #1 (C)	U	Sense Element #2 Excitn.
H	Controller Output #1 (E)	V	Sense Element #2 Excitn.
J	Sense Element #1 Excitn.	W	Not connected
K	Sense Element #1 Excitn.	X	Not connected
L	Equipment Ground	Y	Not connected
M	AC-	Z	Not connected
---	(keyed)		

Figure 6-2: MODEL 228 DUAL-SLOT MAGNETOMETER BOARD EDGE CONNECTOR PIN ASSIGNMENTS

6.3.3.2 MODEL 228 SINGLE-SLOT MAGNETOMETER BOARD EDGE CONNECTOR PIN ASSIGNMENTS (C)=Collector (E)=Emitter

PIN	FUNCTION	PIN	FUNCTION
A	DC Ground	N	AC+
B	+24 VDC	P	Not connected
---	(Keyed)		
C	Detector Reset	R	Not connected
D	Sensing Element #1 Input	S	Not connected
E	Sensing Element #2 Input	T	Not connected
F	Controller Output #1 (C)	U	Not connected
H	Controller Output #1 (E)	V	Not connected
J	Sense Element #1,2 Excitn.	W	Controller Output #2 (C)
K	Sense Element #1,2 Excitn.	X	Controller Output #2 (E)
L	Equipment Ground	Y	Not connected
M	AC-	Z	Not connected
---	(Keyed)		

Figure 6-3: MODEL 228 SINGLE-SLOT MAGNETOMETER BOARD EDGE CONNECTOR PIN ASSIGNMENTS

6.3.4 **FUNCTIONAL REQUIREMENTS: MODEL 227**

6.3.4.1 Each magnetometer detector-sensing element shall be designed to be compatible with the Magnetometer Detector Sensor Unit Model 228.

6.3.4.2 The sensing element shall be cylindrical in shape, shall be no larger than 2.0 inches in diameter or more than 4.0 inches in length and shall contain no moving parts.

6.3.4.3 The sensing element shall have a non-ferrous, moisture-proof housing, shall not be affected by extremes of temperature or humidity, shall be capable of withstanding all types of soil conditions and shall be sealed to prevent the entrance of moisture.

6.3.4.4 The connecting cable attached to each sensing element shall be suitable for both direct burial in earth and installation in conduit, and shall be 50 feet in length, minimum.

Section 4 MODEL 232 MAGNETIC DETECTOR and MODEL 231 SENSING ELEMENT

6.4.1 **GENERAL**

6.4.1.1 The Model 232 shall detect an induced voltage caused by any MOVING vehicle (traveling at all speeds between 3 and 80 Miles per Hour) passing within 6 feet of the Model 231 Sensing Element with 1000 feet of lead-in cable.

6.4.1.2 A single control knob for adjusting the sensitivity of each channel shall be readily adjustable without use of tools and shall be mounted on the front panel.

6.4.1.3 MODEL 232 MAGNETIC DETECTOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS (C)=Collector (E)=Emitter

PIN	FUNCTION	PIN	FUNCTION
A	DC Ground	N	AC+
B	+24 VDC	P	Not connected
---	(Keyed)		
C	Detector Reset	R	Not connected
D	Sensor #1 Input	S	Not connected
E	Sensor #1 Input	T	Not connected
F	Controller Output #1 (C)	U	Not connected
H	Controller Output #1 (E)	V	Not connected
J	Sensor #2 Input	W	Controller Output #2 (C)
K	Sensor #2 Input	X	Controller Output #2 (E)
L	Equipment Ground	Y	Not connected
M	AC-	Z	Not connected
---	(Keyed)		

Figure 6-4: MODEL 232 MAGNETIC DETECTOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS

6.4.2 **FUNCTIONAL REQUIREMENTS: MODEL 231**

6.4.2.1 Each sensing element shall be designed for ease of installation, repositioning, and removal. It shall be no larger than 2.25 inches in diameter and shall have no sharp edges along its length. The overall length shall not exceed 21 inches.

6.4.2.2 Each sensing element including lead-in shall have a DC resistance of less than 3500 ohms.

6.4.2.3 The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a minimum of 50 feet lead-in cable. Leakage resistance shall be a minimum of 10 Megohms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt water bath after the device has been entirely immersed in the bath for a period of 24 hours at 20 (±3) degrees Centigrade. The salt-water bath concentrate shall be one-fourth ounce of salt per gallon of water.

Section 5 MODEL 242 DC ISOLATOR

6.5.1 **GENERAL**

6.5.1.1 The Model 242 Two-Channel DC Isolator module design shall be such that all specification criteria are met without the use of adjustable components.

6.5.1.2 The Model 242 shall contain two channels that provide isolation between electrical contacts external to the module and the controller unit input circuits. The method of isolation shall be based upon a design that provides reliable operation.

6.5.1.3 Each isolation channel shall have a front panel mounted test switch to simulate a valid input. Activation of the test switch shall provide a complete test of the circuitry associated with that channel. The test switch shall be a single pole-double throw, three-position switch providing ON-OFF-Momentary ON positions. An indicator for each channel shall provide a visual indication of a valid channel output.

6.5.1.4 Power failure or power restoration shall not cause an isolator channel output.

6.5.1.5 The isolator shall have an internal power supply, which shall supply 20 (±4) VDC to the field input side of the isolation channels. The isolator shall not draw more than 2.5 watts of AC power. No current shall be drawn from the cabinet D.C. power supply.

6.5.1.6 A channel contact closure input of 5 msec or less shall not cause an output. An input duration of 25 msec or greater shall cause an output. An input duration between 5 msec and 25 msec may or may not cause an output. The channel shall reset within 25 msec after opening of either field contact or test switch.

6.5.1.7 Each isolation channel output shall be turned on (true) when a contact closure causes an input voltage of less than 8 VDC, and shall be turned off (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA or more than 40 mA to an electrical contact closure or short from the power supply.

6.5.1.8 The minimum isolation shall be 1000 Megohms and 2,500 VDC measured between the input and output of the same channel.

6.5.1.9 Electrical or physical damage to the AC power transformer shall not cause further damage to the PC board, or other components on the board.

6.5.1.10 MODEL 242 DC ISOLATOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS (C)=Collector (E)=Emitter

PIN	FUNCTION	PIN	FUNCTION
A	DC Ground	N	AC+
B	+24 VDC	P	Not connected
---	(Keyed)		
C	Not connected	R	Not connected
D	Input #1	S	Not connected
E	Input #1 Common	T	Not connected
F	Controller Output #1 (C)	U	Not connected
H	Controller Output #1 (E)	V	Not connected
J	Input #2	W	Controller Output #2 (C)
K	Input #2 Common	X	Controller Output #2 (E)
L	Equipment Ground	Y	Not connected
M	AC-	Z	Not connected
---	(Keyed)		
NOTE: Pins E & K shall be tied together on the PCB.			

Figure 6-5: MODEL 242 DC ISOLATOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS

Section 6 MODEL 252 AC ISOLATORS

6.6.1 **GENERAL**

6.6.1.1 The Model 252 Two-Channel AC Isolator module design shall be such that all specification criteria are met without the use of adjustable components.

6.6.1.2 The Model 252 shall contain two channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits. The method of isolation shall be based upon a design that provides reliable operation.

6.6.1.3 Each isolation channel shall have a front panel mounted test switch to simulate a valid input. Activation of the test switch shall provide a complete test of the circuitry associated with that channel. The test switch shall be a single pole-double throw, three-position switch providing ON-OFF-Momentary ON positions. An indicator for each channel shall provide a visual indication of a valid channel output.

6.6.1.4 Power failure or power restoration shall not cause an isolator channel output.

6.6.1.5 A channel-input voltage of 80 (±5) VAC (= Von) applied for a duration of 115-(±15) msec shall cause a ground true channel output.

6.6.1.6 The channel output shall be turned off (false) when the input voltage drops 10 VAC or more below its input voltage (Voff = Von – 10 VAC) for a period of 115 (±15) msec.

6.6.1.7 Each channel-input circuit shall have an input impedance between 8000 and 15000 ohms at 60 hertz.

6.6.1.8 The minimum isolation shall be 1000 Megohms between the input and output terminals at 500 VAC applied voltage.

6.6.1.9 MODEL 252 AC ISOLATOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS (C)=Collector (E)=Emitter

PIN	FUNCTION	PIN	FUNCTION
A	DC Ground	N	Not connected
B	+24 VDC	P	Not connected
---	(Keyed)	C	Not connected
R	Not connected		
D	Input #1	S	Not connected
E	Input #1 Common	T	Not connected
F	Controller Output #1 (C)	U	Not connected
H	Controller Output #1 (E)	V	Not connected
J	Input #2	W	Controller Output #2 (C)
K	Input #2 Common	X	Controller Output #2 (E)
L	Equipment Ground	Y	Not connected
M	Not connected	Z	Not connected
---	(Keyed)		

Figure 6-6: MODEL 252 AC ISOLATOR BOARD EDGE CONNECTOR PIN ASSIGNMENTS

CHAPTER 7 MODEL 33x CONTROLLER CABINETS

Section 1 GENERAL / CONFIGURATION

7.1.1 Unless otherwise specified, cabinets shall be furnished, ready for operation, with a Model 210P Conflict Monitor, in the following configurations:

7.1.1.1 ☼ The Power Supply Assembly is incorporated into each Power Distribution Assembly #2. The County may occasionally specify Power Distribution Assembly #1 on Plans or Purchase Orders, which will require the separate Power Supply Assembly to be furnished.

7.1.1.2 ► Provide one Model 242 DC Isolator for Stop Time / Flash Sense in addition to any requested on Plans or Purchase Orders.

7.1.1.3 Model 332 Cabinet (State 332A Configuration) shall consist of:

Housing #1	Output File #1
Mounting Cage #1	C1 Harness #1
☼ Power Distribution Assembly #2	Service Panel #1
Input Files I & J	Input Panel #1
☼ Power Supply Assembly	► Model 242 DC Isolator

7.1.1.4 Model 336 Cabinet (State 336A Configuration) shall consist of:

Housing #2	Output File #1
Mounting Cage #2	C1 Harness #3
☼ Power Distribution Assembly #2	Service Panel #2
Input File I	Input Panel #4
☼ Power Supply Assembly	► Model 242 DC Isolator

7.1.1.5 Model 337 Cabinet shall consist of:

Housing #3	Integral Output File
Integral Mounting Cage	C1 Harness #4
Power Distribution Assembly #337	Integrated Service Panel
Integrated Input File	

7.1.2 All assemblies and files shall be mounted on the cage mounting rails per cabinet model detail. Cabinet model interface wiring shall be per specified C1 Harness; detailed wiring lists and required One Line Wiring Diagram.

7.1.3 **CABINET SHIPPING REQUIREMENTS:** Cabinets shall be delivered mounted on plywood shipping pallets (see plans). The pallets shall be bolted to the cabinet base. The cabinet shall be enclosed in a slipcover cardboard packing shell. The cabinet doors shall be blocked to prevent movement during transportation.

7.1.4 **CABINET ADAPTERS**: When specified, adapters shall be provided. The adapter shall be fabricated of the same material and finish as the cabinet (see plans).

7.1.5 All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

7.1.6 A cage mounting clear area for the controller unit shall be provided. The area shall extend 1.5 inches in front of and 16 inches behind the front EIA mounting angles.

7.1.7 All conductors, terminals, and parts, which could be hazardous to maintenance personnel, shall be protected with suitable insulating material.

Section 2 CABINET HOUSING

7.2.1 The housing shall include, but not be limited to, the following:

Enclosure	Police Panel
Doors	Ventilation
Latches	Locks
Gasketing	Light Fixture
Hinges and Door Catches	Cage Supports and Mounting

7.2.2 **CABINET CONSTRUCTION**

7.2.2.1 The cabinet shall be rainproof with the top of the enclosure crowned a minimum of ½ inch to prevent standing water. It shall have single front and rear doors, each equipped with a lock. When each door is closed and latched, the door shall be locked.

7.2.2.2 The enclosure, doors, lifting eyes, side panels, gasket channels, police panel, and all supports welded to the enclosure and doors shall be fabricated of 0.125 inch minimum thickness aluminum sheet, conforming to the requirements of ASTM designation: B 209 for 5052-H32 aluminum sheet. Bolted on supports shall be both the same material and thickness as the enclosure, or 0.105-inch minimum steel.

7.2.2.3 The bottom of the Model 337 cabinet shall be constructed of material that is at least twice the minimum thickness of the sides, top, or back. The bottom shall also be reinforced in such a manner as to provide solid support for the entire weight of the cabinet assembly, fully equipped, on a pedestal-mount adaptor. The cabinet base layout as shown on the plans, shall accommodate a standard 4-inch pedestal adaptor.

7.2.2.4 All exterior seams for enclosure and doors shall be continuously welded. All welds shall be smooth, and of equal or greater thickness than the base metal after all grinding and smoothing is completed. All edges shall be filed to a radius of 0.03125-inch minimum. Exterior cabinet welds shall be done by the gas tungsten arc (TIG) process only. Internal cabinet welds shall be done by either the gas metal arc (MIG) or gas tungsten arc (TIG) process. ER53556 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum.

7.2.2.5 All construction shall be free of dents, scratches, weld burn-troughs and abrasions harmful to the strength and general appearance.

7.2.2.6 ALUMINUM SURFACES shall conform to the following:

7.2.2.6.1 An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning and etching procedure shall be to immerse in inhibited alkaline cleaner at 71 degrees Celsius for 5 minutes (Oakite 61A, Diversey 909 or equivalent in a mixture of 6 to 8 ounces per gallon of distilled water). Rinse in cold water. Etch in a sodium solution at 66 degrees Celsius for 15 minutes (0.5 ounce sodium fluoride plus 5 ounces of sodium hydroxide mixed per gallon of distilled water). Rinse in cold water. De-smut in a 50% by volume nitric acid solution at 20 degrees C for 2 minutes. Rinse in cold water.

7.2.2.6.2 The anodic coating shall conform to MIL-A-8625C (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, Class I Coating except that the outer cabinet surface coating shall have a 0.0007-inch minimum thickness and 27 milligrams per square inch minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution of nickel acetate (PH 5.0 to 6.5) for 15 minutes at 99 degrees Celsius.

7.2.2.6.3 The County, at its option, may require the winning bidder or contractor to submit written certification of compliance to the requirements listed in this Section.

7.2.2.7 The enclosure door frames shall be double flanged out on all 4 sides and shall have strikers to hold tension on and form a firm seal between the door gasketing and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 0.156 (±0.080) inch.

7.2.2.8 Gasketing shall be provided on all door openings and shall be dust tight. Gaskets shall be 0.25 inch minimum thickness closed cell neoprene or silicone, (BOYD R-10480 or equal), and shall be permanently

bonded to the metal. If neoprene is used, the mating surface of the gasketing shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A Gasket Top Channel shall be provided to support the top gasket on the door to prevent gasket gravitational fatigue.

7.2.2.9 Models 332 and 336: cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness; 0.188 inch if aluminum or 0.105 if steel.

7.2.2.10 All cabinets shall be provided with two removable lifting eyes for placing the cabinet on its foundation. The lifting eyes shall be located to provide reasonable balance when the cabinet is lifted. Each eye opening shall have a minimum diameter of 0.75 inch. Each eye, and its associated mounting hardware, shall be able to support a weight load of 1000 pounds for Models 332 and 336, and 350 pounds for Model 337.

7.2.2.11 All exterior bolt heads shall be of the tamper-proof type.

7.2.2.12 PEDESTAL ADAPTER: Model 337: Each cabinet shall be provided with a bronze standard collar slip-fitter, with straight top, for mounting fabricated aluminum cabinets on a pedestal with 4.5-inch outside diameter standard.

7.2.3 **DOOR LATCHES AND LOCKS**

7.2.3.1 The latching handles shall have provision for padlocking in the closed position. Each handle shall be 0.75-inch minimum diameter stainless steel with a minimum 0.5-inch diameter stainless steel shank. The padlocking attachment shall be placed at 4.0 inches from the handle shank center to clear the lock and key. An additional 4.0 inches minimum gripping length shall be provided.

7.2.3.2 The latching mechanism incorporated into Models 332 and 336 shall be a three-point draw roller type.

7.2.3.2.1 The push-rods shall be turned edgewise at the outward supports and have a cross section of 0.25 inch thick by 0.75 inch wide, minimum. Rollers shall have a minimum diameter of 0.875 inches and shall be equipped with ball bearings and nylon wheels.

7.2.3.3 MODEL 337: The latching mechanism shall be a three-point draw type - rollers are not required.

7.2.3.3.1 The push rods shall be .25-inch diameter minimum stainless steel, and shall be supported within 1.5 inches of their respective striker.

7.2.3.4 When the door is closed and latched, the door shall be locked. The locks and handles shall be on the right side of the front door and the left side of the rear door. The lock support shall be rigidly mounted on the door. Two stainless steel machine screws shall be used to attach the lock to the support. In the locked position, the bolt throw shall extend a minimum of 0.25 (±0.03125) inch into the latch cam area. A seal shall be provided to prevent dust or water entry through the lock opening.

7.2.3.5 Cabinet locks shall be solid brass rim type compatible with Best 5L-series with interchangeable cores. Refer to the current APPROVED EQUIPMENT GUIDE for potential sources.

REFERENCE:	Best Lock	Olympus Lock
Front Door—	5L7RL4XA7559-606	725RD-DR-LH
Rear Door—	5L7RL3XA7559-606	725RD-DR-RH

7.2.3.5.1 Each cabinet shall be supplied with two door locks, each with a temporary construction core, keyed alike to the standard factory construction core combination. Two keys shall be supplied in each cabinet: one "Operating" and one "Control"

7.2.3.5.2 Keys shall be removable in the locked position only. The front portion of the lock shall neither be recessed nor shall it extend more than .1875 inch from the face of the door. The locks shall be mounted on the door in such a position that the tumblers are in the upper quadrant.

7.2.3.6 The locks shall have rectangular, spring loaded bolts. The bolts shall have a 0.281-inch throw and shall be 0.75 inches wide by 0.375 inches thick (tolerance is ±0.035 inch).

7.2.3.7 MODELS 332 and 336: The center latch cam shall be fabricated of a minimum thickness 0.1875 inch plated steel, minimum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved TOWARD the center of the door.

7.2.3.8 MODEL 337: The center latch cam shall be fabricated of a minimum thickness 0.074 inch plated steel, and structured to only allow the door to open when the handle is moved AWAY from the center of the door.

7.2.4 The cabinet ventilation, including intake, exhaust, filtration, fan assembly and environmental control are as follows:

7.2.4.1 The front door shall be provided with louvered vents. The louvered vent depth shall be a maximum of 0.25 inches to minimize vandal and water entry. A pleated-media type air filter shall be provided behind the door vents. The filter filtration area shall cover the vent opening area such that no incoming air shall bypasses the filter. The filter shall be held firmly in place with a bottom bracket and a spring loaded upper clamp. The bottom filter bracket shall be formed into a waterproof sump with drain holes to the outside.

7.2.4.1.1 MODELS 332 and 336: The filter shall be 16 inches wide by 12 inches high by 0.8750 inches thick.

7.2.4.1.1.1 A filter shell shall be provided that fits over the filter to provide mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides shall be bent-over a minimum of 0.25 inches to house the filter.

7.2.4.1.2 MODEL 337: The filter shall be 8 inches wide by 15 inches high by 0.875 inches thick.

7.2.4.2 The intake (including filter) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for Model 332 and 26 cubic feet of air per minute for Models 336 and 337.

7.2.4.3 Cabinets shall be equipped with an electric fan with ball or roller bearings and a capacity of at least 100 cubic feet of free air delivery per minute. The fan shall be mounted within the cabinet and vented.

7.2.4.4 The fan shall be thermostatically controlled and shall be manually adjustable to turn on between 33 degrees Celsius and 65 degrees Celsius with a differential of not more than 6 degrees Celsius between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor amp capacity. The manual adjustment shall be graded in 10 degrees Celsius increment scale.

7.2.5 **HINGES AND DOOR CATCHES**

7.2.5.1 Stainless steel hinges, with two bolts per leaf, shall be provided to bolt the door to the enclosure. Model 332 shall have four hinges, Model 336 shall have three hinges, and Model 337 shall have two hinges. Each hinge shall be 3.5 inches minimum length and have a fixed pin. The pin ends shall be welded to the hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

7.2.5.2 Front and rear doors shall be provided with catches to hold the door open at both 90 and 180 ±10) degrees. The catches shall be capable of holding the door open at 90 degrees in a 60 mph wind acting at an angle perpendicular to the plane of the door.

7.2.5.2.1 MODELS 332 and 336: The catch minimum diameter shall be 0.375 inch for plated steel or aluminum rods, or 0.25 inch stainless steel.

7.2.5.2.2 MODEL 337: 0.25 inch stainless steel rods shall be used. Provisions shall be made to ensure that it would require a conscious act [on the part of the person opening the door] to open it more than 90 degrees.

7.2.6 **DOCUMENTATION ENVELOPE and HANGERS**

7.2.6.1 Documentation envelopes, as described herein, shall be supplied by the vendor. The envelopes shall be the side opening "zip" type, fabricated of heavy-duty clear plastic, measuring 10 x 14 (±1.0) inches. Two 3/8-inch (hole size) grommets shall be mounted on each envelope, spaced 12 5/8 inches center-to-center.

7.2.6.2 MODEL 332: means shall be provided on the front door to hang two separate plastic envelopes, as described in the previous section.

7.2.6.3 MODELS 336 and 337: means shall be provided to hang a plastic envelope on both the front and rear doors.

7.2.6.4 The hanging apparatus and plastic envelopes shall be located so as not to interfere with any of the interior cabinet mechanical or electrical mechanisms.

7.2.7 **POLICE PANEL**

7.2.7.1 A police panel assembly shall be provided to allow the police officers limited access to intersection control.

7.2.7.2 The police panel door shall be equipped with a lock. The lock shall be keyed for a master police key. One key shall be furnished with each police lock. Each police key shall have a shaft at least 1.75 inches in length.

7.2.7.3 The police panel shall contain two DPST toggle switches with contacts rated for 15 amperes at 120 VAC.

7.2.7.4 MODELS 332 and 336: One switch shall be labeled "ON-OFF" and the other "FLASH/AUTOMATIC". The police panel assembly including switches shall not extend into the cabinet more than 1.5 inches.

7.2.7.4.1 The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

7.2.7.4.2 The panel assembly shall have a drain to prevent water collecting within the assembly. The drain shall be channeled to the outside.

7.2.7.5 MODEL 337: One switch shall be labeled "Signals Off" and the other "Auto/Flash". Switches shall be mounted on the front of the Power Distribution Assembly, with access through the front door, as shown on the plans.

Section 3 CABINET CAGE / RACK

7.3.1 Two controller-supporting angles shall be provided along each side of the cabinet. The angles shall be formed from an approved stock, and designed to support a minimum of 50 pounds each. The horizontal side of each angle shall be 3 inches. The angles shall be mounted 17.5 inches from the top of the mounting area for a Model 332 cabinet (adjustable vertically to any position), and 7.25 inches for Model 336 and 337 cabinets.

7.3.2 **MODELS 332 AND 336 CABINET CAGE REQUIREMENTS**

7.3.2.1 A standard EIA 19-inch rack cage shall be installed inside the cabinet for mounting of the controller unit and cabinet assemblies.

7.3.2.2 The EIA rack portion of the cage shall consist of two pairs of continuous adjustable equipment mounting angles. The angle nominal thickness shall be either 0.1345-inch plated steel or 0.105 Stainless Steel. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angle shall comply with Standard EIA RS-310-B and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.

7.3.2.3 Clearance between rails for mounting assemblies shall be 17.75 inches.

7.3.2.4 The cage shall be bolted to each side of the cabinet at 4 points, via the cabinet cage supports and associated spacer brackets, two at the top and two at the bottom of the rails.

7.3.3 **MODEL 337 CABINET RACK REQUIREMENTS**

7.3.3.1 The Rack Assembly shall be self-supporting, and shall allow an open space between the side panels and beneath the lowest horizontal surface (with both cabinet doors closed) of a minimum of 17 inches wide by 16 inches deep by 9 inches high.

7.3.3.2 The assembly shall be equipped with mounting "ears" to allow mounting to standard EIA rails. Overall-width of the assembly shall conform to Standard EIA RS-310-C.

7.3.3.3 The Rack Assembly shall be fabricated and mounted according to the dimensions shown on the plans.

7.3.3.4 The Rack Assembly shall provide a space, which shall intermate with, and support a Model 204 Flasher. The flasher shall be wired as shown on the plans, with its load balanced among load switches 1 through 4.

7.3.3.5 An Auto/Flash switch shall be provided for the use of Maintenance Personnel.

7.3.3.6 Means shall be provided to supply emergency power to the flasher and flash transfer relays in the event that the Power-Distribution Assembly is removed from the rack. This shall be accomplished in a manner, which prevents the application of emergency power unless the maintenance Auto/Flash switch is in the Flash position. Emergency power to the flasher and transfer relays shall be independently protected.

7.3.3.7 The Rack Assembly shall provide a receptacle, which shall intermate with and support the Power Distribution Assembly (PDA). The receptacle shall be equipped with a connector (BEAU SG 5413 ABT or equal). Dimensions for the connector shall be as shown on the plans. Means shall be provided to secure the PDA into the rack assembly.

7.3.3.8 The front face of all plug-in assemblies shall be flush with the front face of the Rack Assembly. The sole exception shall be the Flash Relay, which may be mounted with its socket on the same plane as the flash transfer relay sockets. The front face of the Rack Assembly may be inset from the EIA rails a maximum of ½-inch.

7.3.3.9 The assembly shall allow air circulation from bottom to top.

7.3.3.10 Field wire terminal blocks and bus bars shall be mounted on the back panel of the assembly. The three signal output terminal blocks shall be mounted vertically and shall be the six-position type. The power line service terminal block and bus bars shall be mounted as shown on the plans. The rear panel shall be hinged to allow it to swing down and provide access to terminals, relays, and connections as detailed elsewhere in the specifications, and on the plans.

7.3.3.11 The Rack Assembly shall provide for an Input File sub-assembly and an Output File sub-assembly, both of which shall be integral to the Rack Assembly as shown on the plans and specified in detail under separate headings.

Section 4 CABINET ASSEMBLIES

7.4.1 **GENERAL**

7.4.1.1 The following equipment shall be completely removable from the Models 332 and 336 cabinet without removing any other equipment and using only a slotted or Phillips screw driver:

Power Supply Assembly
Power Distribution Assembly
Input File
Output File
Monitor Unit Assembly

7.4.1.2 All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

7.4.1.3 All equipment in the cabinet, when required, shall be clearly and permanently labeled. The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed. Cabinet environmental conditions shall not adversely affect marker strip material or message visibility.

7.4.1.4 Resistor-capacitor transient suppression shall be provided at all AC relay sockets (across relay coil), except for the Flash Transfer Relays in the output file, where one suppression device may be common for all.

7.4.1.5 A leakage resistor, which permits a small amount of current to pass through the heavy-duty relay coil, shall be installed across the terminals of relay sockets to overcome residual magnetism.

7.4.1.6 Assembly or file depth dimension shall include terminal blocks.

7.4.1.7 All assemblies and files shall allow air circulation through its top and bottom unless specified otherwise.

7.4.1.8 Socket types for the following equipment shall be: (or equal)

Load Switch	BEAU S-5412-LAB
Heavy Duty Relay	BEAU S-5408-LAB
Flasher Unit & Power Supply Module	BEAU 2-5406-LAB
210P Monitor Unit	PCB 28/56S

7.4.1.9 Connector sockets for Flasher Unit, Power Supply, and Load Switch modules shall be mounted with their front face 7.5 inches deep from assembly or file front panel.

7.4.1.10 Guides (top and bottom) shall be provided for Load Switch, Flasher Units, Monitor Units, Detector and Isolator Modules and Power Supply Module (bottom only). The guides shall begin 1.0 (±0.5) inch in from the front panel surface and extend to within 0.5 inches of the connector socket face.

7.4.1.11 Assemblies and Files shall be fabricated of 0.080-inch minimum thickness aluminum or stainless steel sheet. Aluminum shall be Grade 6061, or better, T4 or T6 material. The metal surface shall be treated with clear chromate.

7.4.1.12 If pop rivets are used in fabrication of assemblies or files, they must be stainless steel.

7.4.2 **POWER SUPPLY ASSEMBLY**

7.4.2.1 A power supply shall be provided to supply +24 VDC to the Input and Output Files for use by their associated devices. The power supply shall be of ferro-resonant design having no active components and conform to the following requirements:

7.4.2.1.1 LINE REGULATION: 2% from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1.0% frequency change.

7.4.2.1.2 LOAD REGULATION

7.4.2.1.2.1 Models 332 and 336 cabinets: 5% from 1 ampere to 5 amperes with a maximum temperature rise of 30 degrees Celsius above ambient.

7.4.2.1.2.2 Model 337 cabinet: 5% from 1 ampere to 3 amperes with a maximum temperature rise of 30 degrees Celsius above ambient.

7.4.2.1.3 Design voltage: +24 ± .5) VDC at full load, 30 degrees C, 115 VAC line voltage after a 30 minute warm-up period. No-load voltage shall not exceed +27 VDC.

7.4.2.1.4 FULL LOAD CURRENT

7.4.2.1.4.1 Models 332 and 336 cabinets: 5 amperes, minimum.

7.4.2.1.4.2 Model 337 cabinet: 3 amperes, minimum.

7.4.2.1.5 Ripple / Noise: 2 Volts peak-to-peak and 500 millivolts RMS at full load. (Maximum)

7.4.2.1.6 Line Voltage: 90 to 135 VAC

7.4.2.1.7 Efficiency: 70% minimum

7.4.2.1.8 Minimum Voltage: +22.8 VDC

7.4.2.1.9 Power Supply Circuit capacitors shall be rated for 40 volts, minimum.

7.4.2.2 When Power Distribution Assembly #1 option is requested, the power supply assembly in Models 332 and 336 cabinets shall utilize no more than 3 ½ inches of rack height, and a maximum depth of 5 ½ inches. Power Supply Assembly wiring in Model 332 shall facilitate easy relocation to the rear rails.

7.4.2.3 The front panel shall include, but not be limited to:

7.4.2.3.1 All fuses or circuit breakers, properly labeled;

7.4.2.3.2 Power-ON indicator for D.C. Output, labeled "24VDC PWR";

7.4.2.3.3 Power-ON indicator for A.C. Input, labeled "AC Power";

7.4.2.3.4 Test points or meter for monitoring the output D.C. voltage.

7.4.2.4 Power-On indicators and the D.C. Voltage test points shall be on the protected side of their respective fuses or circuit breakers.

7.4.2.5 The assembly including terminals shall be protected to prevent accidentall contact with energized parts.

7.4.2.6 The power supply cage and transformer shall be securely braced to prevent damage in transit.

7.4.3 **POWER DISTRIBUTION ASSEMBLIES (PDA**)

7.4.4 The following equipment shall be provided with the power distribution assemblies:

7.4.4.1 PDA #1:

	PDA #1 (County)
1 EA	Duplex NEMA 5-15R Controller Receptacle (rear panel)
2 EA	Duplex NEMA 5-15R Equipment Receptacle (one with GFI, located on the front panel, and one located on the rear panel)
1 EA	Single Pole 50 Amperes Main Circuit Breaker
1 EA	Single Pole 15 Amperes 120 VAC Equipment Circuit Breaker
4 EA	Single Pole Signals Circuit Breakers 15 Amperes, 120 VAC, with Auxiliary Switch feature and Curve 3 Trip characteristics
1 EA	2 Pole Ganged 20 Amperes 120 VAC Flash Bus Circuit Breaker
1 EA	Mercury Contactor rated 60 Amperes, minimum, 120 VAC
2 EA	Model 204 Flasher Units and Sockets
1 EA	Auto/Flash Switch
1 EA	FLASH Indicator
1 EA	10 position Terminal Blocks T1 & T2

7.4.4.2 PDA #2

	PDA #2 (County)
1 EA	Duplex NEMA 5 15R Controller Receptacle
2 EA	Duplex NEMA 5 15 R Equipment Receptacles (one with GFI)
1 EA	Single Pole 50 Amperes 120 VAC Main Circuit Breaker
*4 EA	Single Pole Signals Circuit Breakers 15 Amperes, 120 VAC, with Auxiliary Switch feature and Curve 3 Trip characteristics
1 EA	2 Pole Ganged 20 Amperes 120 VAC Flash Bus Circuit Breaker
1 EA	Mercury Contactor rated 60 Amperes, minimum, 120 VAC
2 EA	Model 204 Flasher Units and Sockets
1 EA	Model 206 Power Supply Module and Socket
1 EA	Auto/Flash Switch
1 EA	FLASH ON Indicator
3 EA	10 position Terminal Blocks T1, T2, and T4
1 EA	4 position Terminal Block T3
*	or optionally...
6 EA	Single Pole Signals Circuit Breakers 15 Amperes, 120 VAC, with Auxiliary Switch feature and Curve 3 Trip characteristics

7.4.4.3 Rating of breakers shall be shown on face of breaker or handle. Breaker function shall be labeled below breakers on front panel.

7.4.4.4 The Signals Circuit Breakers, with the auxiliary switch feature shall be wired as shown in the Plans. The breaker auxiliary switch circuit shall be open when the breaker is in the ON position. The auxiliary circuits shall be wired in parallel, so that any tripped breaker shall energize the Mercury Contactor Coil, Flash Transfer Relay Coils, and the "FLASH" Indicator. The auxiliary switch contacts shall be rated at 5 amperes, 120 VAC, minimum. The auxiliary switch circuit terminals shall be soldered.

7.4.4.5 The first equipment receptacle in the circuit shall have ground-fault circuit interruption as defined in the National Electrical Code. Circuit interruption shall occur with 6 mA of ground-fault current and shall not occur with less than 4 mA of ground-fault current.

7.4.4.6 An "Auto/Flash" switch shall be provided which, when placed in "Flash" position (down), shall energize the Mercury Contactor (MC) Coil. When the switch is placed in the "Auto" position, (up) the Load switches shall control the signal indications. The switch shall be an SPST toggle switch rated for 15 amperes at 120 VAC.

7.4.4.7 A lamp labeled "Flash Operation" shall be provided on the assembly's front panel. The lamp shall be driven by flasher #1/ output #1 through Flash Relay Circuit No. 1, or per Circuit Breaker option.

7.4.4.8 All conductors from the power distribution assembly routed to the cabinet wiring shall be connected to the terminal block on the common side, except for the AC power conductor between the service terminal block and main circuit breaker. All internal conductors terminating at the blocks shall be connected to the other side of the blocks.

7.4.4.9 Terminal screw size shall be 10-32 for terminal blocks T1, T2, and T4, and 6-32 for terminal block T3.

7.4.4.10 MODEL 206 POWER SUPPLY

7.4.4.10.1 The Model 206 Power Supply Module shall meet the requirements specified in section 7.4.2.1and 7.4.2.3

7.4.4.10.2 The module chassis shall be vented. Its top and sides shall be open except for unit supports.

7.4.4.10.3 When resident in the PDA Assembly, the module shall be held firmly in place by a stud screw, assembly connector support panel, and a wing nut.

7.4.4.10.4 Surge Network: Two 0.5 ohm, 10 watt minimum, wire-wound power resistors with a 0.2 µH inductance shall be provided (1 on the AC+ power line, and 1 on the AC line). Three MOV surge arrestors, rated for 50 Joules, minimum, shall be supplied between AC and Equipment Ground, AC and Equipment Ground,

and between AC and AC. A 0.68 µF capacitor shall be placed across AC and AC between the two power resistors and the MOV's.

7.4.4.11 PDA #337 (County)

7.4.4.11.1 The PDA #337 shall be furnished and installed in the Rack Assembly. Maximum dimensions are 12.05 inches wide by 3.9 inches high by 7.375 inches deep. It shall be equipped with a connector to inter-mate with its associated connector in the Rack Assembly. Pin assignments shall be as shown on the plans.

7.4.4.11.2 The following equipment shall be provided with the PDA #337:

1 EA	Single Pole 30 Amperes 120 VAC Main Circuit Breaker *
1 EA	Single Pole 15 Amperes 120 VAC Equipment Circuit Breaker *
1 EA	Single Pole 30 Amperes 120 VAC Signals Circuit Breaker *
1 EA	Single Pole 15 Amperes 120 VAC Flasher Circuit Breaker *
1 EA	24 VDC Power Supply
1 EA	Power Relay and socket
1 EA	Auto/Flash Switch (Police)
1 EA	Signals Off Switch
1 EA	Power Indicator
1 EA	Flash Indicator
2 EA	24 VDC Power Supply Test Points
2 EA	Power Supply Fuses (AC and DC)

The circuit breaker characteristic shall be as follows:
Main - TRIP CURVE 2
Equipment - TRIP CURVE 3
Signals - TRIP CURVE 3
Flasher - TRIP CURVE 3

7.4.4.11.3 The Auto/Flash switch, when placed in "Flash" position, shall energize the Power Relay coil and apply a stop-time input to the controller. When the switch is placed in the "Auto" position (up), the load switches shall control the signal indications. The switch shall be a double-pole/ single-throw, rated for 15 amperes at 120 volts AC.

7.4.4.11.4 The Signals-Off switch, when placed in the "Off" position (down), shall energize the Power Relay coil and interrupt power to the flasher. The switch shall be a three-pole/double-throw, rated for 15 amperes at 120 volts AC. Two of the three poles shall be tied in parallel to provide sufficient switching capacity for flasher power.

7.4.4.11.5 The Power Indicator shall be a 24-volt DC lamp tied across the Power Supply output on the fused side.

7.4.4.11.6 The Flash Indicator shall be a 120-volt AC lamp tied across the Power Relay coil.

7.4.4.11.7 The Power Relay shall be a Model 430 relay wired as shown on the plans. When the relay is energized, it shall interrupt power to the load switches.

7.4.5 **INPUT FILE**

7.4.5.1 The file shall have a maximum depth of 8.5 inches and shall intermate with, and support 14 two-channel detector sensor or isolator units in the 332 and 336 cabinets, and 11 two-channel detector sensor or isolator units in the 337 cabinet.

7.4.5.2 The file shall provide a PCB 22/44S connector centered vertically for each two-channel detector. The associated number and letter side connectors shall be shorted internally. Pins D, E, F, J, K, L, and W shall be brought out to an 8-position terminal block on the back of the file (one spare terminal). The output emitters shall be common grounded with the ground terminating at TB-15, Position 4 in 332 and 336 cabinets, and IF-15 Position 4 in 337 cabinets. Position 8 of the terminal block is assigned to Equipment Ground (Pin L) and is used to terminate leads with shields.

7.4.5.3 The Input File shall have PCBA card guides both top and bottom. The card guides shall begin 1.0 (±0.5) inch back from the front face of the file.

7.4.5.4 The Input File shall be provided with marker strips along the top and bottom to identify isolators and detectors in the file.

7.4.5.5 Terminal screw size for Input File Terminals shall be 8-32.

7.4.6 **OUTPUT FILE**

7.4.6.1 GENERAL REQUIREMENTS

7.4.6.1.1 All circuits in the Output File shall be individually wired. Printed circuit motherboards shall not be used in the Output File. No. 14 (minimum) stranded wire shall be used from the load switch connector pins to the field terminals, including wiring to the Flash Transfer Relays.

7.4.6.1.2 All cabinets shall be directly wired to flash all vehicle phases red.

7.4.6.1.3 Plastic or nylon guides (top and bottom) shall be provided to support the conflict monitor unit.

7.4.6.1.4 The controller unit outputs to the Output File shall be connected as follows:

7.4.6.1.5 Models 332 and 336: through Connector C4, as shown on the plans.

7.4.6.1.6 Model 337: directly wired to the Output File.

7.4.6.1.7 The Output File shall be provided with marker strips to identify load switches when mounted in the file.

7.4.6.1.8 The Monitor socket connector shall be a PCB 28/56S.

7.4.6.1.9 All conflict monitor channel green and yellow inputs shall be wired, with unconnected channel wires labeled and tied back in a bundle. Tied-back wires shall be of sufficient length to connect to any output file terminal.

7.4.6.1.10 It shall be possible to remove the monitoring device without causing the intersection to go into flashing operation. The cabinet shall be wired so that if the front cabinet door is closed with the monitor unit removed, the intersection shall go into flashing operation (See One Line Diagram). The cabinet shall contain a conspicuous warning against operation with the monitor unit removed.

7.4.6.1.11 Load switch connectors, monitor unit connectors, and flash transfer relay sockets shall be accessible from the back of the Output File without the use of tools or removal of any other equipment.

7.4.6.1.12 Field wire terminal blocks shall be mounted vertically on the back of the assembly. Output File #1 (332 and 336 cabinets), shall have 3 terminal blocks with 12 positions, and Output File #2 (337 cabinets), shall have 3 terminal blocks with 6 positions. Output file terminal screw size shall be 10-32.

7.4.6.1.13 The Flash Transfer Relays shall be Heavy Duty Type. The coil of relay shall be energized only when the signals are in flashing operation and the police panel ON/OFF switch is ON. The relay shall transfer the field outputs from load switch output to flash control. The transfer shall not interrupt the controller unit operation.

7.4.6.1.14 The depth of the file shall not exceed 14.5 inches.

7.4.6.2 RED MONITORING INTERFACE

7.4.6.2.1 All 332, 336, and 337 cabinets shall be equipped with a Red Monitoring Interface, mounted integrally with the Output File, on the back panel, or mounted near the output file and accessible from the rear of the cabinet.

7.4.6.2.2 All associated wiring, connectors, and circuit boards shall provide adequate labeling.

7.4.6.2.3 The red outputs from each load switch shall be wired to a connector, designated as P20, which interfaces to the Model 210P Conflict Monitor via a ribbon cable 24 (±2) inches in length.

7.4.6.2.4 P20 Connector Pin Assignments shall be as follows:

PIN	FUNCTION	TERMINAL BLOCK	PIN	FUNCTION	TERMINAL BLOCK
1	Channel 15 Red	15	11	Channel 9 Red	9
2	Channel 16 Red	16	12	Channel 8 Red	8
3	Channel 14 Red	14	13	Channel 7 Red	7
* 4	Chassis Ground	17	14	Channel 6 Red	6
5	Channel 13 Red	13	15	Channel 5 Red	5
* 6	Special Func.2	18	16	Channel 4 Red	4
7	Channel 12 Red	12	17	Channel 3 Red	3
* 8	Special Func.1	19	18	Channel 2 Red	2
9	Channel 10 Red	10	19	Channel 1 Red	1
10	Channel 11 Red	11	20	Red Enable	20
* Red Monitoring Special Functions					

Figure 7-1: P20 Connector Pin Assignments.

7.4.6.2.5 Keying shall be between pins 3 & 5, and 17 & 19 (the odd numbered pins are on one side, and the even pins are on the other). The P20 connector and the CMU connector shall be keyed physically alike to prevent the Red Monitoring cable from being inserted into the P20 180 degrees out of alignment.

7.4.6.2.6 RED ENABLE INPUT

7.4.6.2.6.1 Pin 20 of the Red Monitoring Connector shall provide the Red Enable input to the monitor. Red Enable is a 120 VAC input to the conflict monitor that enables additional monitoring functions. Source for Red Enable shall be TB01 terminal 1 in the 332 and 336 cabinets, and FR (Flash Relay) pin 6 in the 337 cabinet.

7.4.6.2.7 Special Function 1 and 2 Inputs

7.4.6.2.7.1 Pin 8, (Special Function 1), is for future use

7.4.6.2.7.2 Pin 6, (Special Function 2), is for future use.

7.4.6.3 OUTPUT FILE #1: 332 and 336 Cabinets

7.4.6.3.1 The output file shall be capable of containing 12 Model 200 Load Switches, 4 Flash Transfer Relays, and the Model 210P Monitor Unit. Four Flash Transfer Relays and one Model 210P Monitor Unit shall be furnished with each output file.

7.4.6.3.2 The monitor unit compartment, (including the housed Model 210P Monitor Unit, exclusive of handle), shall extend no farther than 1.25 inches in front of the 19 inch rack front surface. The load switch socket connector front surface shall be no more than 8.5 inches in depth from the front surface of the output file.

7.4.6.3.3 Conflict Monitor channels 9 and 10 shall be wired as follows:

CMU Channel	Field Terminal
9 YELLOW	105
9 GREEN	114
10 YELLOW	111
10 GREEN	120

7.4.6.4 OUTPUT FILE #2: 337 Cabinets

7.4.6.5 The Model 337 output file shall be capable of containing six Model 200 load switches, three Model 430 flash transfer relays, one Model 210P conflict monitor unit, and one Flash Relay.

7.4.6.6 Provision shall be made via jumper or connector to connect load switch 5 yellow and load switch 6 yellow to conflict monitor channel 7 yellow and channel 7 green respectively, in addition to their standard connections to channels 5 and 6. The means of connection shall be readily accessible with the output file rear panel open.

7.4.6.7 The sockets for each load switch, flash transfer relay, and monitor unit, shall be accessible from the back of the file without the use of tools.

7.4.6.8 AUXILIARY OUTPUT FILE: Model 420

7.4.6.8.1 The Auxiliary Output File shall; accommodate six Model 200 Load Switches and be provided with two Flash Transfer Relays.

7.4.6.8.2 All circuits in the Auxiliary Output File shall be individually wired. Printed circuit motherboards shall not be used in the Auxiliary Output File. No. 14 (minimum) stranded wire shall be used from the load switch connector pins to the field terminals, including wiring to the Flash Transfer Relays.

7.4.6.8.3 All Auxiliary Output Files shall be directly wired. to flash Load Switches No. 1, 2, 4, and 5 red.

7.4.6.8.4 The controller unit outputs. to the Auxiliary Output File shall be connected through Connector C5, as shown on the plans.

7.4.6.9 HEAVY DUTY RELAY: Model 430

7.4.6.9.1 Heavy-duty relays shall be the electro-mechanical type designed for continuous duty.

7.4.6.9.2 Each relay shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating and part number shall be written clearly and permanently on the cover.

7.4.6.9.3 Each relay shall be provided with DPDT contacts. Contact points shall be of fine silver, silver alloy, or superior alternative material. Contact points and arms shall be capable of switching a 20 ampere at 120 VAC tungsten load per contact once every 2 seconds with a 50% duty cycle for at least 250,000 operations without contact welding or excessive burning, pitting, or cavitation.

7.4.6.9.4 The relay coils power consumption shall be 10 volt-amperes or less.

7.4.6.9.5 Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a 1 cycle surge rating of 175 amperes RMS.

7.4.6.9.6 SIDE PANELS: 332 and 336 cabinets

7.4.6.9.6.1 Two panels shall be provided and mounted on the cage parallel to the cabinet sides. In viewing from the back door, the left side panel shall be designated as the "Input Panel" and the right side panel shall be designated as the "Service Panel".

7.4.6.10 CABINET HARNESSES

7.4.6.10.1 The C1 Harness shall be a minimum of 4 feet in length. The harness wire bundle shall be provided with external protection and routed on the Input Panel Side of the cabinet. Sufficient length shall be provided to allow the C1P Connector to properly connect any approved Model 170 Controller Unit mounted in the cabinet.

7.4.6.10.2 One end of the C1 Harness shall be the C1P Connector with pin contacts wired per the detail assignment. The other ends of the harnesses shall terminate as follows:

7.4.6.10.2.1 332 Cabinet: C4S Connector (connected to C4P on Output File #1)

7.4.6.10.2.1.1 C5S Connector (connected to C5P on either the Input Panel or the Auxiliary Output File, Model 420 Assigned Input Files I & J Positions and Logic Ground Bus

7.4.6.10.2.2 336 Cabinet: C4S Connector (same as Harness #1)

7.4.6.10.2.2.1 Assigned Input File I Positions, Input Panel Terminal Block and Logic Ground Bus

7.4.6.10.2.3 337 Cabinet: (no connector)

7.4.6.10.2.3.1 Assigned Input File I Positions, Input Panel Terminal Block, Load Switch connectors and Logic Ground Bus

7.4.6.10.3 Conductors between the C1 Connector and the Input File (s) shall be of sufficient length to allow any conductor to be connected to any detector output terminal (Positions S, F, or W).

7.4.6.11 CABINET LIGHT REQUIREMENTS

7.4.6.11.1 Cabinet Light fixtures shall be connected to the cabinet wiring harnesses via an appropriate connector, to facilitate replacement of the entire fixture without disconnecting or desoldering wires.

7.4.6.11.2 Each 332 and 336 cabinet shall be equipped with one (1) fluorescent Sentinel lighting fixture Model No. SL20A10RS mounted inside the top portion of the cabinet from front to rear. Any fixture other than the specified unit shall be submitted to the County for approval, prior to the delivery of the sample unit. The fixture shall have an F-15-T-8 cool white lamp; operated from a normal power factor, U.L. listed ballast. An R-C type surge suppressor shall be SOLDERED across the AC+ and neutral leads as close to the primary side of the ballast as practical. Door actuated switches shall be installed to turn the cabinet light on when either front or rear door is opened. The door switches shall be on a separate circuit; and used only to turn on the cabinet light.

7.4.6.11.3 Each 337 cabinet shall be equipped with a fluorescent lighting fixture mounted inside the top rear of the cabinet. The fixture shall have an eight (8) watt lamp AT5-CW, operated from a normal power factor, U.L. listed Ballast. The lamp shall be shaded to diffuse the light. A door-actuated switch shall be installed to turn the cabinet light on when either front or rear door is opened.

Section 5 CABINET WIRING

7.5.1 All cabinet wiring shall be neat, firm, and routed to minimize crosstalk and electrical interference.

7.5.2 **CABINET WIRING DIAGRAM**

7.5.2.1 Four sets of non-fading (comparable to Xerox 2080) cabinet wiring diagrams shall be supplied with each cabinet. The diagrams shall be nonproprietary. They shall accurately identify all cabinet circuitry in such a manner as to be readily interpreted. The cabinet drawing shall show the equipment layout in an elevation view as viewed from the rear of the cabinet with the left and right cabinet walls shown in their relative positions. The diagrams shall be placed in the plastic pouch and attached to the front cabinet door.

7.5.2.2 Two cabinet manuals shall be provided in the pouch together with the wiring diagram sets.

7.5.3 **CONDUCTORS**

7.5.3.1 All crimp and compression terminals shall be applied **ONLY** to bare wire. Solder **ONLY** after crimping. All conductors used in cabinet wiring shall terminate with properly sized non-insulated or clear insulated spring-spade type terminals except when soldered to a through-panel solder lug on the rear side of the terminal block or as specified otherwise. If non-insulated terminals are used, they shall be used for DC logic-level terminations only. All crimp-style connectors shall be applied with a properly aligned and adjusted power tool, (as recommended by the manufacturer of the terminals), which prevents opening of the handles until the crimp is completed.

7.5.3.2 Crimp-type connectors shall **NOT** be used on solid wires within any assembly unless the connector is both crimped and soldered.

7.5.3.3 Conductors between the service terminal AC- and Equipment Ground and their associated bus, the equipment ground bus conductor to Power Distribution Assembly and cage rail, AC Bus to Power Distribution Assembly shall be No. 8 or larger.

7.5.3.4 All conductors unless otherwise specified shall be No. 22, or larger, with a minimum of 19 copper strands. Conductors shall conform to Military Specification: MIL-W-16878D, Type B, or better. The insulation shall have a minimum thickness of 10 mils and shall be nylon jacketed polyvinyl chloride except that Conductors No. 14 and larger may have Type THHN insulation (without nylon jacket), and shall be stranded with a minimum of 7 copper strands.

7.5.3.5 All conductors, except those that can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

7.5.3.6 All conductors shall conform to the following COLOR-CODE requirements.

7.5.3.6.1 The grounded conductors of AC circuits shall be identified by a continuous white or gray color.

7.5.3.6.2 The equipment grounding conductors shall be identified by a solid green color or by a continuous green color with 1 or more yellow stripes.

7.5.3.6.3 The DC logic ground conductors shall be identified by a solid white color with a red stripe.

7.5.3.6.4 The ungrounded AC+ conductors shall be identified by a solid black or black with colored stripe.

7.5.3.6.5 The Logic ungrounded conductors shall be color coded differently from those circuits carrying AC voltages.

7.5.3.6.6 Other conductors shall be identified by any color not specified above.

7.5.3.7 All wiring harnesses shall be neat, firm and routed to minimize crosstalk and electrical interference. Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring, EXCEPT IN THE OUTPUT FILE. (see paragraph 7.4.6.1.1)

7.5.3.7.1 Wiring containing AC shall be routed and bundled separately or shielded separately from all logic voltage control circuits.

7.5.3.7.2 Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

7.5.3.8 Within the cabinet, the DC logic ground and equipment ground shall be electrically isolated from the AC grounded conductor and each other by 500 Megohms when tested at 250 VDC, with the power line surge protector disconnected.

7.5.3.9 The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 0.25 inch shall be used for securing the bus to the service panel.

7.5.3.10 The cabinet power supply DC Ground shall be connected to the DC logic ground bus using a No. 14, or larger, stranded copper wire.

7.5.3.11 Each detector lead-in pair, from the field terminals in the cabinet to the sensor unit rack connector, shall be a cable of UL Type 2092 or better, and shall have terminals that are both crimped and soldered. The stranded tinned copper drain wire shall be connected to a copper equipment grounding bus located on the Input Panel.

7.5.4 **TERMINAL BLOCKS**

7.5.4.1 The terminal blocks shall be barrier type rated at 20 amperes, 600 volts RMS minimum. The terminal screws shall be 0.3125 inch minimum length, nickel plated brass, standard machined slot binder head type (neither stamped nor a combination slot-Phillips), with screw inserts of same material. Screw size is specified under associated cabinet assembly, file or side panel.

7.5.4.2 Round inserts shall not be used in any terminal blocks without specific County approval.

7.5.4.3 Screw inserts and screws shall be designed to meet the following minimum torque requirements:

6-32	8 in-lbs
8-32	16 in-lbs
10-32	25 in-lbs

7.5.4.4 INPUT PANEL TERMINAL BLOCKS: Each input panel terminal block provided for field wire termination of detector inputs shall be a Kulka #602-GP-12-SLB (or approved equivalent). Each terminal block shall be a 12-position eyelet constructed type, engaging a minimum of 3½ threads per terminal, mounted with an insulating strip if an open-back design. A marker strip may be used as an insulating strip.

7.5.4.5 POWER LINE SERVICE TERMINAL BLOCK: The terminals of the power line service terminal block shall be labeled "L1" and "AC-", and shall be covered with a clear insulating material to prevent inadvertent contact. Terminating lugs large enough to accommodate No. 2 conductors shall be furnished for the service terminal block.

7.5.4.5.1 MODELS 332 and 337: Service Terminal Block, Marathon #1423307, or approved equal, shall be provided.

7.5.4.5.2 MODEL 336: The terminal block shall be rated for 50 amperes at 600 volts peak, minimum. The block shall be either a double row, 3 position screw/insert with shorting bar (screws, inserts and shorting bars shall be nickel plated brass) or a Marathon #1423307 (or approved equal). If the Marathon block is used, the surge protectors shall be terminated under a screw head (not common with AC+, AC, or Equipment Ground). The AC, AC-, and Equipment Ground conductors connecting to the service terminals and appropriate busses shall not be spade lugged.

Section 6 POWER LINE SURGE PROTECTION

7.6.1 Two types of power line surge protectors shall be provided between both line conductors (AC+ and AC) and equipment ground. The protectors shall be installed at the service terminal block.

7.6.2 If terminal lugs are used on the leads of the devices, they shall be crimped and soldered.

7.6.3 One type of surge protector shall be the Three-Electrode Gas Tube Type and shall have the following ratings:

IMPULSE BREAKDOWN: Less than 1,000 volts in less than 0.1 µsec at 10 kilovolts/µsec.
STANDBY CURRENT: Less than 1 mA.
STRIKING VOLTAGE: Greater than 212 VDC.
Capable of withstanding 15 pulses of peak current each of which will rise in 8 µsec and fall in 20 µsec to 0.5 of the peak voltage at 3 minute intervals. Peak current rating shall be 20,000 amperes.

7.6.4 The other type of surge protector shall be Metal Oxide Varistor (MOV). One shall be installed between AC+ and equipment ground and the other between AC and equipment ground. The MOV shall have the following ratings:

RECURRENT PEAK VOLTAGE: 212 Volts
ENERGY RATING MINIMUM: 50 Joules
POWER DISSIPATION: Average 0.85 Watt
PEAK CURRENT FOR PULSES: 2,000 Amperes for less than 6 µsec
STANDBY CURRENT: Less than 1 mA

CHAPTER 8 RADIO TIME BASE and ACCESSORIES

Section 1 - SCOPE

8.1.1 This specification covers radio receiving equipment designed to receive and decode Coordinated Universal Time data that is transmitted from the Global Positioning System, Stations WWV, and/or WWVH

8.1.2 A The Traffic Signal Controller is connected to a serial RS232C port (providing date and time data) or to a resynchronization pulse output (a pulse provided once per day at a preselected time).

Section 2 GENERAL

8.2.1 Unit designs that vary from this specification, but are functionally equivalent, may be submitted to the County for evaluation.

8.2.1.1 Los Angeles County Department of Public Works Traffic Signal Test Facility must approve, in advance, **ANY** changes to the equipment supplied by a Vendor under any existing Purchase Agreement or Project Contract.

8.2.2 Each unit supplied under this specification must meet the following criteria:

8.2.2.1 Each unit must be compatible with all Los Angeles County software written specifically to decode Time and Date information from WWV Receiver Units.

8.2.2.2 Each unit must be certified to comply with the limits for a Class B computing device pursuant to Subpart J of Part 15 of the FCC Rules.

8.2.2.3 Unit Power shall be supplied from the Traffic Signal Controller or from an external power supply.

8.2.2.4 If powered from the Traffic Signal Controller, the power shall be supplied from pin 9 of the DB9 Connector, and be +5 Volts DC, with maximum current of 200 ma.

8.2.2.5 If an external power supply is needed, each unit must be supplied with a computer grade power supply with over-voltage and over-current protection that meets or exceeds existing equipment performance.

8.2.3 The County remains the sole judge on the ability of each device to meet Specifications.

Section 3 FUNCTIONAL

8.3.1 **SYSTEM OPERATION**

8.3.1.1 Each Receiver supplied shall communicate bidirectionally through a 3-wire serial RS-232C interface (configured as DCE) using the standard 7-bit ASCII character set. The communications format shall utilize 1 Start bit, 1 Stop bit, and be selectable between 7-bit/even parity and 8-bit/no parity. The command set MUST include, but is not limited to;

8.3.1.1.1 **S or SET Commands:**

8.3.1.1.1.1 **"SBn"** sets the serial port baud rate (bit rate).

n	is an ASCII character in the range "0" to "8".
0	not used, was 110 baud.
1	not used, was 300 baud.
2	not used, was 600 baud.
3	1200 baud.
4	2400 baud.
5	4800 baud.
6	9600 baud.
7	19200 baud.
8	38400 baud.

8.3.1.1.1.2 **"SDn"** enables or disables automatic daylight-saving time correction.

n	can be either 1 or 0.
0	disables daylight-saving time correction.
1	enables daylight-saving time correction.

8.3.1.1.1.3 **"SMn"** sets the output format for the time to be either 12 hour format (AM/PM) or 24 hour format ("military").

n	can be either 1 or 0.
0	sets the output to 24 hour format.
1	sets the output to 12 hour format (AM/PM).

8.3.1.1.1.4 **"SNn"** sets the newline character. The default newline character shall be the ASCII carriage return (CR).

n	any ASCII character except colon and /. The default is caracter return (CR).

8.3.1.1.1.5 **"SOn"** sets the time zone offset.

n	is an ASCII chaeacter in the set, "0 1 2 3 4 5 6 7 8 9 : ; < = > ? @ A B C D E F G" to set the time zone betwen 0 and 23. Note, the operand character to send can be computed by adding 48 (the ASCII code for 0) to the time zone. Do not include the daylight-saving time correction.
0	Time zone 0 or UTC.
5	Time zone 5 or Eastern Time.
6	Time zone 6 or Central Time.
7	Time zone 7 or Mountain Time.
8	Time zone 8 or Pacific Time (default)
9	Time zone 9 or Alaska Time
:	Time zone 10 or Hawaii Time.

8.3.1.1.2 **Q or Query Commands:**

8.3.1.1.2.1 "**QD**" Query Date returns the date where:

Format	"YY/MM/DD/doy<CR>" or “NOT LOCKED ON” if the verification phase has not been completed.
YY	is the last two digits of the year
MM	is the number of the month
DD	is the day of the month
doy	is the day of year (Julian 1-366)
<CR>	is an ASCII carriage return

8.3.1.1.2.2 "**QT**" (Query Time) returns the time.

Format	"mHH:MM:SS.Thtd<CR>" or “NOT LOCKED ON” if the verification phase has not been completed.
m	is A or P, or a space if 24 hr mode
HH	is the hour (2 digits)
MM	is the minute (2 digits)
SS	is the second (2 digits)
T	is the tenths of a second
h	is the hundredths of a second
t	is the thousandths of a second
d	is a D if DST is enabled & in effect, otherwise a space
<CR>	is an ASCII carriage return

8.3.1.1.2.3 "**QH**" (Query Hardware) responds "**abcdef<CR>**" where:

a is not used
b is baud rate
c is DST, 12/24 HR, Time Zone
d is Time Zone
e is not used
f is Time Re-sync hour
<CR> is an ASCII carriage return
Note: QH is used in the older WWV Time Base Units only. It is not used in the newer Type GPS Time Base Units.

8.3.1.1.2.4 "**QM**" (Query Mode) response format varies between the older WWV Time Base Units and the newer GPS Time Base Units:

8.3.1.1.2.4.1 Older WWV only Time-Base Units. Do not use for new designs.

THE FORMAT FOR OLDER WWV TIME BASE UNITS: “FRDZYCCHHSSFTTTTTUU<CR>” WHERE:	
f is enabled frequency	
r is baud rate	
d is daylight saving	
z is Time Zone	
y is year	
cchh is 0	
SS is Bit	
	0 set if signal bad 1 set if hardware fault 2 set if out of spec 3 set if locked on
F is frequency selected	
T is transmitter	
tttt is minutes since last valid time received	
uu is 0	
<CR> is an ASCII carriage return	

8.3.1.1.2.4.2 Newer GPS Time Base Units. Use in new designs.

The format for newer and GPS Time Base Units is “Bn:Dn:M1:Ncr:On<newline>”:	
Bn is Baud Rate number:	
	0 is Reserved. 1 is Reserved. 2 is Reserved. 3 is 1200 4 is 2400 5 is 4800 6 is 9600 (default) is 19200 8 is 38400
Dn is Daylight Savings Time is:	
	0 is Disabled 1 is Enabled (default)
Mn is 12 or 24 hour time format:	
	0 is 24 hour 1 12 hour (default)
Ncr is New Line character set as:	
	Default is <CR>, can be set as any ASCII character except colon and /.
On is Time Zone setting:	
	n is an ASCII chaeacter in the set, “0 1 2 3 4 5 6 7 8 9 : ; < = > ? @ A B C D E F G” to set the time zone between 0 and 23 to where: 0 is UTC. 1 thru 23 is UTC –n. (note): 5 is Eastern (USA). 6 is Central. is Mountian. is Pacific (default) is Alaska or “:” is Hawaii
<newline>	
	newline character as defined above.

8.3.2 **SYSTEM PERFORMANCE**

8.3.2.1 TIME ACCURACY: Shall be to within 10 milliseconds of Coordinated Universal Time (UTC), traceable to the National Institute of Standards and Technology (NIST), formerly known as the National Bureau of Standards.

8.3.2.2 DRIFT (while no signal is being received): Shall be no more than 100 milliseconds per day at room temperature.

8.3.2.3 Acquisition Time: less then 5 min to lock-up.

8.3.3 **RECEIVER / AMPLIFIER SECTION**

8.3.3.1 TYPE: Shall be WWV (AM) and/or GPS receiver.

8.3.3.2 FREQUENCIES: WWV, WWVH; 2.5, 5, 10, 15, and 20 MHZ. GPS; 1.57542 GHz (L1).

8.3.3.3 ANTENNA TO RECEIVER CONNECTION: Shall accept a 50-ohm antenna input through a BNC connector.

8.3.3.4 WWV: SELECTIVITY: Shall have an I.F. bandwidth of 3KHz @ 3dB points.

8.3.3.5 WWV: IMAGE REJECTION: Shall be 60 dB or better.

8.3.3.6 WWV: SENSITIVITY: Shall be 1 microvolt for 20 dB (S+N)/N minimum nominal and shall be audible at less than 0.5 microvolt input.

8.3.3.7 WWV: AUTOMATIC GAIN CONTROL: Shall have less than 1 dB change in audio output for a 90 dB change in input level.

8.3.4 **HARDWARE/SOFTWARE SELECTABLE OPTIONS**

8.3.4.1 WWV: AUDIO OUTPUT: Shall be 1 watt into 8 ohms, with less than 5% distortion (using an external speaker with volume control).

8.3.4.2 BAUD RATE: Shall be software selectable to provide rates of 1200, 2400, 4800, 9600, 19200 and 38400 baud.

8.3.4.3 TIME ZONES: Shall be selectable in 1-hour increments subtracted from UTC (0-23).

8.3.4.4 DAYLIGHT SAVINGS TIME: Shall be selectable as to whether or not to correct for DST.

8.3.4.5 TIME MODE: Shall be selectable between 12 or 24-hour modes.

8.3.4.6 WWV: PROPAGATION DELAY: Shall be correctable from 0 to 43 milliseconds, in 1-millisecond increments (minimum).

Section 4 PHYSICAL and ELECTRICAL

8.4.1 **PHYSICAL SECTION**

8.4.1.1 DIMENSIONS: Shall not exceed 3" high, 9" wide, and 10" deep.

8.4.1.2 WEIGHT: Shall not exceed 5 pounds.

8.4.2 **ELECTRICAL**

8.4.2.1 ALL EQUIPMENT supplied, when wired into existing circuits, shall maintain isolation of external DC Logic Ground, EARTH GROUND, and AC Neutral circuits from each other: 500 Megohms (minimum) when tested at 250 volts DC.

8.4.2.2 POWER: Unit Power shall be supplied from the Traffic Signal Controller or from an external power supply.

8.4.2.3 If powered from the Traffic Signal Controller, the power supplied shall be from pin 9 of the DB9 Connector, be +5 Volts DC, and with a current of 200 ma maximum.

8.4.2.4 If an external power supply is needed, Input power shall be 12-15 volts DC, with a current of 750 ma maximum.

8.4.3 **LIGHTNING PROTECTION**: All equipment shall be supplied with an L.A. County approved lightning arrestor for placement in-line with the antenna lead-in.

Section 5 CONNECTORS

8.5.1 **ANTENNA: BNC 50 OHM ANTENNA CONNECTOR**

8.5.2 J2: DB9 INPUT/OUTPUT PORT (used in older WWV Time Base Units only).

1- Audio Mute Control (ground input)
2- 12-15 Volt DC
3- Ground
4- no connection
5- 6-11 Volt DC input (optional battery)
6- To wiper of Volume potentiometer
7- To top of Volume 5K Audio Taper pot.
8- AGC output to Signal Strength Meter
9- Audio Output to 8 ohm Speaker

8.5.3 **POWER INPUT:**

8.5.3.1 If powered from the Traffic Signal Controller, the power shall be supplied from pin 9 of the DB9 Connector, and be +5 Volts DC, with a current of 200 ma or less.

8.5.3.2 If an external power supply is needed Molex type 39-01-2020 (or equiv.)

1- 12-15 Volt DC input (200-700 mA)
2- Ground

8.5.4 **COMM PORT:**

8.5.4.1 **DB25 RS-232C:** *(was used in older WWV Time Base Units).*

2- Transmit Data (from host computer) (170's C2-K)
3- Receive Data (to host computer) (170's C2-L)
7- Ground (170's C2-N)
8- +5 VDC (from 170 controller) 200 ma maximun. (170's C2-D)
20- Not Used

8.5.4.2 **DB9 RS-232C:**

2- Receive Data (to host computer) (C2-L)
3- Transmit Data (from host computer) (170's C2-K)
5- Ground (170's C2-N)
8- 1PPS (1 Hz)
9- +5 VDC (from 170 controller) 200 ma maximum. (170's C2-D)

8.5.5 Each receiver supplied shall include a 4-foot cable to interface the J4 connector to a Model 170 Traffic Signal Controller C2 connector (AMP 201355-3 [or equivalent] including guide socket near pin A, guide pin near pin P, and associated hardware):

C2: pin	Signal	J4: pin
D	+5 VDC, 200 ma supply. [jumper pin D & H together]	n.c.
H	Carrier Detect [jumper pin H, J & M together]	n.c.
J	Ready To Send	n.c.
M	Clear To Send	n.c.
K	DATA OUT (from 170, to rcvr)	2
L	DATA IN (to 170, from rcvr)	3
N	Signal Ground	7

8.5.6 **J5: DB15 DISPLAY PORT** *(was used in older WWV Time Base Units).*

DB15	Signal
1	Ground
2	
3	
4	
5	1 Hz Pulse Output
6	TTL Level TxD
7	TTL Level RxD
8	
9	12 Volts DC+
10	
11	
12	
13	
14	Time Resync Out
15	

CHAPTER 9 MODEL 2070 CONTROLLER UNIT (2070 UNIT)

Note: This specification is based on the "City of Los Angeles Department of Transportation Model 2070 Controller Specifications" Dated December 2000. The L. A. City's specification is in turn based on Caltrans "TEES" Dated November 1999.

Section 1 GENERAL

9.1.1 **THE 2070 CONTROLLER MUST BE LISTED IN THE CITY OF LOS ANGELES, DEPARTMENT OF TRANSPORTATION'S QPL BEFORE IT IS SUBMITTED TO THE COUNTY.**

9.1.2 **POWER FAILURE and POWER RESTORATION:**

9.1.2.1 **POWER FAILURE:** A power failure is said to have occurred when the incoming line voltage falls below 92 "2) VAC for 50 msec. The determination of the 50 msec interval shall be completed within 67 msec of the time the voltage falls below 92 ("2) VAC.

9.1.2.2 **POWER RESTORATION:** Power is said to be restored when the incoming line voltage equals or exceeds 97 ("2) VAC for 50 msec. The determination of the 50 msec interval shall be completed within 67 msec of the time the voltage first reaches ("2) VAC.

9.1.2.3 The hysteresis between power failure and power restoration voltage settings shall be a minimum of 5 volts and a maximum of 6 volts.

9.1.3 **Reference is made to CHAPTER 1Section 1 (Scope). The County remains the sole Judge on the ability of each device to meet specifications**.

9.1.4 The Controller Unit shall be composed of the UNIT CHASSIS, modules and assemblies. The following is a list of composition deliverables associated to items:

UNIT VERSION	DESCRIPTIVE:
2070 UNIT	Full unit mated to 170 cabinet family
2070N UNIT	Full unit mated to TS1 cabinet family
2070L UNIT LITE	Unit mated to 170 cabinet family
2070LC UNIT LITE	Unit mated to ITS & TS2 cabinet families
2070LCN UNIT LITE	Unit mated to TS1 cabinet Family

9.1.4.1 Modules and assemblies:

ITEM DESCRIPTION		UNIT VERSIONS:				
		2070	2070N	2070L	2070LC	20070LCN
UNIT CHASSIS		1	1	1	1	1
Model 2070-1A	Two Board CPU	1	1	-	-	-
Model 2070-1B	One Board CPU	-	-	1	1	1
Model 2070-2A	Field I/O for 170 Cab	1	1	1	-	-
Model 2070-2B	Field I/O for ITS/NEMA Cab	-	1	-	1	1
Model 2070-3A	Front Panel-Display A	1	1	-	-	-
Model 2070-3B	Front Panel-Display B	-	-	1	-	-
Model 2070-3C	Front Panel-Blank	-	-	-	1	1
Model 2070-4A	Power Supply – 10 AMP	1	1	-	-	-
Model 2070-4B	Power Supply - 3.5 AMP	-	-	1	1	1
Model 2070-5A	VME Cage Assembly	1	1	-	-	-
Model 2070-5B	MCB 1A Mounting Assembly	-			-	
Model 2070-8	NEMA Interface Module	-	1			1
Model 2070-9	2070N Back Cover	-	1			1

Figure 9-1: 2070 MODULES AND ASSEMBILES

9.1.4.2 The communications and option modules/assemblies shall be called out separately from the unit version. The composition weight shall not exceed 11.3 kilograms (25 lbs).

9.1.5 Purchase requisition is for Model 2070 Controllers with a unit version of "2070 UNIT" including:

Unit Chassis
Model 2070-1A
Model 2070-2A
Model 2070-3A
Model 2070-4A
Model 2070-5A
Model 2070-6A, (or, configurable to either 2070-6A or 2070-6B)
Model 2070-7A, (Isolation of signals and ground not required)

9.1.6 Spare Modules: The manufacturer shall provide one complete set of replacement modules for every 100-controller units purchased on a contract. One set of complete replacement modules is listed as following:

Model 2070-1A
Model 2070-2A
Model 2070-3A
Model 2070-4A
Model 2070-6A (or configurable to either 2070-6A or 2070-6B)
Model 2070-7A (isolation of signals and ground not required)

9.1.7 A permanent label, "COUNTY OF LOS ANGELES", shall be stenciled or embosses on the front of the Model 2070 Controller Unit, centered directly above the LCD.

9.1.8 The AUX switch shall be stenciled or embossed on the front of the of the Model 2070 Controller Unit with the words "STOP TIME", centered and to the left of the switch. The word "STOP" can reside directly over the word "TIME" to minimize horizontal space needed.

9.1.9 A manufacturer's unit serial number shall be placed on the chassis on the right side of the power supply, in front of the back plane of the VME buss cage, as viewed from the front.

9.1.10 Documentation: The Manufacturer shall provide one (1) set of manuals and schematics per Unit per purchase contract. The manuals and schematics shall reflect the latest board revisions and changes.

9.1.11 Test Hardware: The manufacturer shall provide five (5) sets of wraparound harnesses, special test jigs, and extender boards for performing diagnostics or repairs. These shall be provided with the first shipment of any new contract on a one-time basis.

9.1.12 The CHASSIS Enclosure, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Cover Plates, Power Supply Enclosure, and Front Panel shall be made of 1.524 mm (1/16 inch) minimum aluminum sheet. Maximum height shall not exceed 178 mm (7 inches).

9.1.13 2070 UNIT module / assembly power limitations shall be as follows:

Models:	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
MCB	750 mA	-----	-----	-----
TRANS BD	750 mA	-----	-----	-----
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A&B FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	100 mA	-----	50 mA	50 mA
2070-5 VME Cage	5.0 A	-----	200 mA	200 mA
2070-6 All Comm	500 mA	-----	100 mA	100 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA

Figure 9-2: 2070 MODULE/ASSEMBLY POWER LIMITATIONS

9.1.14 All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 megabits per second. Isolation circuitry shall be by opto- or capacitive-coupled isolation technologies.

9.1.15 The EIA-485 Line Drivers/Receivers shall be socket mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARDS control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1- RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

9.1.16 A Mean-Time-Between-Failure Analysis Report shall be provided with the Qualified Products List Submittal. It shall encompass the 2070 Unit (complete) and its individual modules / assemblies. The report shall describe in detail the methodology used.

9.1.17 Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9.1.18 SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

	SP 5	SP3
CPU 2070-1	“ 19"	“19”
FI/O 2070-2A & -8	" 20"	“NA”
CPU Broadcast to all	"127"	“255”

Figure 9-3: SP5 & SP3 FRAME ADDRESS ASSIGNMENTS

9.1.19 The AGENCY reserves all other addresses. The SDLC response frame address shall be the same address as the Command frame it receives.

Section 2 MODEL 2070-1 CPU MODULE

9.2.1 The MODEL 2070-1A CPU shall consist of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

9.2.2 The MODEL 2070-1B CPU shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the MOTHERBOARD Slot A5. The module shall meet all the requirements listed under this section and Chapter Details Section 7 except for the following:

9.2.2.1 The VME software and hardware bus requirements shall not apply nor do the MCB and Board Interface Harness physical requirements.

9.2.2.2 A Dual SCC Device (asynch/synch) and associated circuitry shall be furnished to provide two additional system serial ports.

9.2.2.2.1 The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1.

9.2.2.2.2 The Dual SCC2 shall be assigned as System Serial Port SP8.

9.2.2.2.3 The SP8 and associated circuitry shall interface with the MC68360 address and data structure and serially be connected to the external world via the DB 25-Pin, C13S Connector located on the module front panel.

9.2.2.2.4 The SP8 shall meet all SP2 Port requirements including EIA 485 drivers/receivers and synchronous bps rate of 614 Kbps.

9.2.2.2.5 A internal LOGIC Switch shall be provided to disconnect SP8 RTS, CTS and DCD (Pins 5, 6,7,18,19 and 20) lines from C13S Connector.

9.2.2.3 The 68360 SCC1 shall be reassigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802-3 (TP) 10 BASE T Standard Requirements, both hardware and software.

9.2.2.3.1 The four network lines shall be used to route ETHERNET across the MOTHERBOARD to the “A” Connectors.

9.2.2.3.2 DC Grounding plane around the network connectors and lines shall be provided.

9.2.2.3.3 Network Lines shall be assigned as:

Network 1 = ENET TX+
Network 2 = ENET TX-
Network 3 = ENET RX+
Network 4 = ENET RX-

9.2.2.3.4 In addition, the conditioned ETHERNET shall be brought out on RJ 45 C14S Connector mounted on the CPU-1B Front Panel.

9.2.2.3.5 Four LED’s labeled “TX, RX, TX Collision, and TX Status” shall be mounted on the front panel signifying ETHERNET operational conditions.

9.2.2.4 The 2070-1B CPU shall not draw more than 1.25 A of +5VDC & 500 mA of ISO+12 VDC.

9.2.3 **MAIN CONTROLLER BOARD (MCB)**

9.2.3.1 The MCB shall be a 3U VME bus compliant board. The MCB shall contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester and BTO (64).

9.2.3.2 The CONTROLLER Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for AGENCY use only. The Interrupts shall be configured as follows:

9.2.3.2.1 (See 9.2.3.2) Addition: An ACFAIL event shall generate a fast IRQ interrupt vectored to auto vector 31. Priority 1 to 3 of the auto vector 31 shall be reserved for user programs. Interrupt service with higher priority shall not clear interrupt flag to allow OS9 to propagate the ACFAIL interrupt.

Level 7	VMEbus IRQ7, ACFAIL
Level 6	VMEbus IRQ6
Level 5	VMEbus IRQ5, CPU Module Counters / Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4	VMEbus IRQ4
Level 3	VMEbus IRQ3
Level 2	VMEbus IRQ2
Level 1	VMEbus IRQ1

9.2.3.3 MEMORY ADDRESS ORGANIZATION

8000 0000 - 80FF FFFF	STANDARD
9000 0000 - 9000 FFFF	SHORT

9.2.3.3.1 Sixteen (16) megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's RBF Manager. The address of each memory block shall be specified by the Contractor and provided with the documentation.

9.2.3.3.2 When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. A on-board circuit shall sense the +5 VDC Standby Power and shift to a On-board CPU Power source. The CPU On-board Power shall be capable of holding the SRAM and TOD Clock up for 30 Days. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

9.2.3.4 RAM MEMORY

9.2.3.4.1 A minimum of 4 MB of DRAM, organized in 32-bit words, shall be provided.

9.2.3.4.2 A minimum of 512 KB of SRAM, organized in 16- or 32-bit words, shall be provided. The SRAM shall draw no more than 50 μA at +5 VDC in Standby Mode.

9.2.3.4.3 The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the time of acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

9.2.3.5 FLASH MEMORY – A minimum of 4 MB of FLASH Memory, organized in 16- or 32-bit words, shall be provided.

9.2.3.5.1 The MCB shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control.

9.2.3.5.2 No more than 1 MB of FLASH Memory shall be used for Boot Image (List) and a minimum of 3 MB shall be available for AGENCY use.

9.2.3.6 TIME-OF-DAY CLOCK: A software settable hardware Time-of-Day (TOD) clock shall be provided.

9.2.3.6.1 It shall, under on-board standby power, operate for a minimum of 30 days maintaining an accuracy of ±1 minute per 30 days at 25° C.

9.2.3.6.2 The clock shall be aliened to a minimum fractional second resolution of 10 ms and shall track seconds, minutes, hours, day of month, month, and year.

9.2.3.7 A software-driven CPU RESET signal (Active LOW) shall be provided to reset other controller systems.

9.2.3.7.1 The signal output shall be driver capable of sinking 30 mA at 30 VDC.

9.2.3.7.2 Execution of the program module “CPURESET” in the boot image shall assert the CPU RESET signal once.

9.2.3.8 An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity LED INDICATOR.

9.2.3.9 The OS-9 Operating System TICK Timer shall be derived from the each transition of LINESYNC with a tick rate of 120 ticks per second.

9.2.4 A TRANSITION Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Motherboard.

9.2.4.1 Said signal and communication lines shall be driven/received off and on the module compliant to EIA- 485.

9.2.4.2 The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 &A3 INSTALLED lines.

9.2.4.3 If the DC Ground is not present (slot not occupied) at the CPU EIA- 485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

9.2.5 A SHIELDED INTERFACE HARNESS shall be provided.

9.2.5.1 It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors.

9.2.5.2 A minimum of 25 mm of slack shall be provided.

9.2.5.3 No power shall be routed through the harness.

9.2.5.4 The harness shall be 100% covered by an aluminum Mylar foil and an extruded black 0.8 mm PVC jacket or equal.

9.2.6 DATA KEY -A DATAKEY Receptacle (KC4210, KC4210PCB or equal) with Key (DK1000or equal) resident shall be provided and mounted on the CPU module front panel (or the Transition Board of Model 1A).

9.2.6.1 The Black DATAKEY shall be tested, interrogated and all 128 addresses read using Software Interface.

9.2.6.2 Power shall not be applied to the receptacle if the key is not present.

9.2.7 **CPU MODULE SOFTWARE:** The following shall be supplied:

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Error Handler
5. Validation Suite
6. Deliverables

9.2.7.1 OPERATING SYSTEM: The CPU Module shall be supplied with Microware Embedded OS-9 Version 3.03 or later software and, in addition, the following:

1. Embedded OS-9 Real Time Kernel
2. Sequential Character File Manager (SCFMAN)
3. Sequential Protocol File Manager (SPFMAN)
4. Pipe File Manager (PIPEMAN)
5. Random Block File Manager (RBFMAN)
6. C Input Output Library (CIO)

9.2.7.2 Boot Image shall include the following utility modules:

break	date	deiniz	devs	free	copy
dir	tmode	edt	list	load	deldir
dump	del	ident	iniz	irqs	events
echo	kill	dcheck	cio	link	kermit
lmm	mdir	mfree	pd	makdir	save
attr	rename	procs	unlink	sleep	xmode
shell	build	setime			

Figure 9-4: BOOT IMAGE UTILITY MODULES

9.2.7.3 DRIVERS AND DESCRIPTORS

9.2.7.3.1 Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

9.2.7.3.2 Drivers shall be provided to access the FLASH, SRAM, and DRAM memories through RBFMAN. The following RBFMAN descriptors shall apply:

d0	Floppy Diskette Drive	Reserved name; no driver required
/f0	FLASH Drive	Accessed as RAM disk & OS-9 /dd default Device
/h0	Hard Disk Drive	Reserved name; no drive required
/r0	SRAM Drive	Accessed as RAM disk
/r1		Reserved; no driver required
/r2	Temporary DRAM Drive	Allows 1 MB of DRAM, accessed as RAM disk; not initialized at boot time

Figure 9-5: RBFMAN DESCRIPTORS

9.2.7.3.3 This section is optional at the vendor's choice (internal timers). A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Access to the MC68360 internal timers shall be through SCFMAN using the following descriptors:

9.2.7.3.3.1 Descriptor names for each timer:

timer 1 = access to MC68360's internal timer #1
timer2 = access to MC68360's internal timer #2
timer3 = access to MC68360's internal timer #3
timer4 = access to MC68360's internal timer #4
timer12 = access to MC68360's internal timer #1 & #2 [cascaded]
timer34 = access to MC68360's internal timer #3 & #4 [cascaded]

9.2.7.3.3.2 Timer descriptor option structure: The driver shall change appropriate timer functions only and ignore values that do not apply to a particular timer function. The data structure is as follows:

```
typedef struct {

    // Timer Global Configuration Register Related Options:
      rserveTGCR :11 ;(MSB)
      timerCAS   :1  ; // Cascade timers
      timerFRZ   :1  ; // Freeze
      timerSTP   :1  ; // Stop timer
      timerRST   :1  ; // Reset timer
      timerGM    :1  ; // Gate mode default = 0 (LSB)

    // Timer Mode Register Related Options:
      timerPS    :8  ; // Prescale value default = 0 (MSB)
      timerCE    :2  ; // Capture vdge & enable interrupts                    default = 0

      timerOM    :1  ; // Output mode default = 0
      timerORI   :1  ; // Output reference interrupt enable default = 0

      timerFRR   :1  ; // Free Run or Restart default = 0
      timerICLK  :2  ; // Input Clock Source default = 1
      timerGE    :1  ; // Gate Enable; default = 0 (LSB)

    // Timer Reference Register
      U_INT16 timerTRR default = 0

    // Timer Capture Register
      U_INT16 timerTCR default = 0xffff

    // Timer Event Register
      reserveTER :14 ; // Reserve (MSB)
      timerREF   :1  ; // Output reference event default = 1
      timerCAP   :1  ; // Capture event default = 1 (LSB)
} TTimer_opts;
```

Figure 9-6: TIMER DESCRIPTOR DATA STRUCTURE

9.2.7.3.3.3 Standard OS-9 SCFMAN Function Calls:

error_code _os_open (char *timer_desc_name, path_id *path);

error_code _os_close (path_id path);

error_code _os_gs_popt (path_id path, u_int32*sizeof(TTimer_opts), void *timer_opts);

error_code _os_ss_popt (path_id path, u_int32*sizeof(TTimer_opts), void *timer_opts);

error_code _os_write (path_id path, void *timer_value, 4);

error_code _os_read (path_id path, void *timer_value, 4);

9.2.7.3.4 The OS-9 SCFMAN shall provide access to the CPU Datakey and its control through the following descriptor name and OS-9 functions:

9.2.7.3.4.1 Descriptor name: datakey =CPU Datakey

9.2.7.3.4.2 Function Calls:

```
error_code_os_open(char*datakey_desc_name, path_id*path);
// error_code= E$NotRdy if CPU Datakey is not installed

error_code_os_read(path_id_path, void*control,128);
//  error_code=E$NotRdy if CPU Datakey is not inserted

error_code_os_close((path_id path);
```

9.2.7.3.5 The async-communications serial device driver shall operate in six modes described below to accommodate communications network (EIA 232) and their associated flow control mode number (FCM #).

FCM#	DESCRIPTION:
0)	No Flow Control Mode: The CTS and CD signals are set asserted internally, so the serial device driver can receive data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. This is the default mode for Model 2070 controllers. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode.
1)	Manual Flow Control Mode: The serial device driver transmits and receives data regardless of the RTS, CTS, and CD states. The user program has absolute control of the RTS state and can inquire of the states of CTS and CD. The states of CTS and CD are set externally by a DCE. The device driver doesn't assert or de-assert the RTS.
2)	Auto-CTS Flow Control Mode: The serial device driver transmits data when CTS is asserted. The CTS state is controlled externally by a DCE. The user program has absolute control of the RTS state. The CD is set asserted internally. The device driver doesn't assert or de-assert the RTS.
3)	Auto-RTS Flow Control Mode: The CTS and CD are set asserted internally. The serial device driver receives and transmits data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. If the user program asserts the RTS, the RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty. Parameters related to delays of the RTS turn-off after last character are user configurable.
4)	Fully Automatic Flow Control Mode: The serial device driver receives data when CD is asserted. Upon a write command, the serial device driver asserts RTS and wait for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed. Parameters related to delays of RTS turn-off after last character are user configurable. If user program asserts the RTS, RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty.
5)	Dynamic Flow Control Mode: The Serial device driver maintains a transmit buffer and a receive buffer with fixed sizes, controls the state of RTS and monitors the state of CTS. The transmission and reception of data are managed automatically by the serial device driver. The serial device driver transmits data when CTS is asserted. The serial device driver asserts RTS when its receiving buffer is filled below certain level (low watermark), and de-asserts RTS when its receiving buffer is filled above certain level (high watermark).

Figure 9-7: ASYNC-COMMUNICATIONS SERIAL DEVICE DRIVER MODES

9.2.7.3.5.1 The serial device driver shall be able to accept user configuration commands to configure the device driver via OS9 _os_ss_size() function call and to accept user request commands for status of serial port from the device driver via OS9 _os_gs_size() function call. The single 32-bit variable passed by _os_ss_size() is defined as follow:

9.2.7.3.5.1.1 Flow Control Code is SS_OFC (0x23):

Bits	Description:
31-24	Auto RTS turn-off extension count in number of characters (range=0-255 1=default).
23-16	Reserved
15	Auto RTS turn-off extension timing (0=bps rate=default, 1=equivalent 1200 bps).
14-13	Reserve for Future Use (default=0).
12	Inhibit Change of SCC MRBLR for opened path (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR for opened path (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range=0-5).
7-0	Flow Control Code (FCC) =0x23
	Note: The RTS turn-off extension can represent a bps rate independent time value rather a number of character times, (higher bps rates are normalized to equivalent 1200 bps characters) when selected by bit 15=1. Thus, a value of 4 represents the time of four characters at 1200 bps even when the actual rate is 9600. If bit 15=0, then an extension value = 4 represents 4 characters, which at a bps rate of 9600 would extend the RTS by approximately 3.3 ms.

Figure 9-8: FLOW CONTROL CODE SS_OFC to _os_gs_size_()

9.2.7.3.5.1.2 Flow Control Code is SS_IFC (0x22):

BITS	DESCRIPTION:
31-22	Flow Control Mode 5 high water mark value (range=1-1023; default=256).
21-12	Flow Control Mode 5 low water mark value (range=1-1023; default=256).
11	Inhibit DCD activating control (default=0; 0=off; 1=on).
10	DCD flow control is active (default=0; 0=NO; 1=YES, changed by FCM#).
9-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC) = 0X22.
	Note: The inhibit DCD selection has priority over the DCD ON request in the same access. Therefore, sending 0x0000022 results in DCD inhibit and DCD Flow Control inactive for all Flow Modes. A new flow control mode number shall set DCD function to that required in the new mode unless DCD is inhibit is ON.

Figure 9-9: FLOW CONTROL CODE SS_IFC to _os_gs_size_()

9.2.7.3.5.1.3 Flow Control Code is SS-Ssig (0x1a):

Bits	Description:
31-16	A signal number to be sent to calling process when the state of a pin is changed.
15-14	Reserved for Future Use (default=0).
13	Ring is asserted (capable hardware only).
12	CTS is de-asserted.
11	CTS is asserted.
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC) = 0x1a.

Figure 9-10: FLOW CONTROL CODE SS-Ssig to _os_gs_size_()

9.2.7.3.5.1.4 Flow Control Code is SS-DCmd (0x0d):

Bits	Description
31-15	Reserved for Future Use (default=0).
14	De-assert DTR (capable hardware only).
13	Assert DTR (capable hardware only).
12	De-assert RTS (duplicated function with _os_ss_DsRTS();).
11	Assert RTS (duplicated function with _os_ss_EnRTS();).
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC)=0x0d.

Figure 9-11: FLOW CONTROL CODE SS-DCmd to _os_gs_size_()

9.2.7.3.5.1.5 The single 32-bit variable returned by _os_gs_size() is defined as follows:

Bits	Description:
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use (default=0).
10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Used (default=0).
6	Overrun error –0=no error; 1=error on last received character.
5	Frame error –0=no error; 1=error on last received character.
4	Parity error –0=no error; 1=error on last received character.
3	Ring state –0=de-asserted; 1=asserted (capable hardware only).
2	DSR state –0=de-asserted; 1=asserted (capable hardware only).
1	DCD state –0=de-asserted; 1=asserted.
0	CTS state –0=de-asserted; 1=asserted.

Figure 9-12: RETURNED VARIABLE from _os_gs_size_()

9.2.7.3.6 Four input buffering modes shall be provided:

1	Line	Characters are buffered up to and including a programmable termination character.
2.	Fixed	A fixed specific number of characters is buffered by the driver.
3.	Timed	Characters are buffered until a programmable inter-character time out occurs.
4.	Raw	Characters are unbuffered and delivered to the task as received.

Figure 9-13: INPUT BUFFERING MODES

9.2.7.3.7 Line, Fixed, and Timed Modes shall be capable of being used together. Raw mode shall disable all other buffering modes.

9.2.7.3.8 Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led	= access to CPU Activity LED Indicator
dstclock	= access to Daylight Savings Time Clock correction

Figure 9-14: CPU LED and DAY LIGHT SAVINGS TIME CORRECTION DEVICE DRIVERS

9.2.7.3.8.1 The standard OS-9 SCFMAN library calls and their functions are as follows:

error_code _os_open (char *desc_name, path_id *path); //open descriptor for command
error_code _os_close (path_id path); //close descriptor

error_code _os_write (path_id path, void *value, 1); //set value or function
*value = 1, turn led on or turn DLSclock feature on (default)
*value = 0, turn led off or turn DLSclock feature off

error_code _os_read (path_id path, void *value, 1); //get current state

Figure 9-15: SCFMAN library calls

9.2.7.3.9 TIME OF DAY (TOD) CLOCK: The OS-9 operating system's TOD Clock shall be driven by the LINESYNC derived OS-9 Operating System TICK Timer. The manufacturer shall provide the following features to support the TOD operation and synchronization.

9.2.7.3.9.1 Leap Year and Daylight Savings Time (DST) Adjustments: The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years. A SCFMAN driver shall be provided to enable/disable the automatic DST adjustment.

9.2.7.3.9.2 Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS- 9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

9.2.7.3.9.3 Setting OS-9 System Clock from Hardware Clock: At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall by synchronized to a minimum of 10 ms resolution.

9.2.7.3.10 The FLASH RAM drive (/f0) shall be protected from corruption due to power failure during a write operation. The current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose. A large file being written, but truncated due to power fail, shall not be restored intact.

9.2.7.4 APPLICATION KERNEL

9.2.7.4.1 The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The initialization routines shall configure the serial port protocols as follows:

SP1 & 2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP 3S	614.4 Kbps (170E-ATC = 153.6 Kbps)
SP4	9.6 Kbps, 8-bit word, 1 stop, no parity, no pause, XDR off, xoff
SP 5S	614.4 Kbps
SP 6	38.4 Kbps, 8-bit word, 1 stop and no parity

Figure 9-16: SERIAL PORT PROTOCOLS

9.2.7.4.2 Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 1.3 seconds.

9.2.7.4.3 A Trap Library routine, "Warmboot," shall be provided, which upon execution shall first shut down the OS-9 operating system, then jump to the start of the initialization routines executed on SYSRESET and proceed.

9.2.7.4.4 After initialization (boot up from SYSRESET), the program shall fork to the defined module in FLASH memory named OPEXEC preceded by a full path. If OPEXEC is not found or fails, the program shall fork a shell. If OPEXEC is forked successfully, the program shall exit.

9.2.7.4.5 A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. A Short Out results in resumption of Application Software without an operating system reboot. The Contractor shall provide a documented method for the Application Software to recover from Level 7 IRQ (ACFAIL) without a SYSRESET. A Long Out is defined as ACFAIL transition to LOW followed by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

9.2.7.5 ERROR HANDLER

9.2.7.5.1 Error handling routine to cope with initialization and power-up test anomalies shall be provided. Errors that occur during initialization and/or during power-up test shall produce a report.

9.2.7.5.2 The Error Handler shall respond to the following conditions and generate an Error Report (saved in Memory):

1. Timer initialization error
2. Timer power up test error
3. Serial communication port initialization error
4. Serial communication port power up test error
5. Peripheral component initialization error

9.2.7.5.3 The Error Handler error report shall contain, at a minimum, component identification and an error code to identify the form of the error. The error report shall be a file accessible through the Random Block File Manager and named "ErrorReport."

9.2.7.6 VALIDATION SUITE

9.2.7.6.1 A validation suite of software and associated documentation shall be provided. It shall include all diagnostic programs necessary to test all 2070 UNIT functions. The diagnostic programs shall demonstrate that all software and hardware functions operate in conformance to specified functionality. It shall provide a working example of how to program all functions

9.2.7.6.2 Validation suite software and associated documentation shall be segmented into individual test sequences. It shall be possible to separate out any one or group of these sequences and, with the addition of a general header file, execute it in isolation or in combination with application software.

9.2.7.6.3 When factory boot code is operating without the User “Opexec” started, the Validation Suite shall be invoked from the front panel keypad, either as a execution in a continuous loop or by individual test selections.

9.2.7.6.4 The validation suite shall execute as a task of the OS-9 Shell Utilities and Commands module. Execution from the shell shall be by typing "Valsuite" from the prompt. If the User Program has been executed, the VALSUITE shall not execute any of its tests due to resource conflicts. It shall be possible to execute the following additional CPU Module specific commands while in the OS-9 Shell Utility:

1. Get/Set the hardware time of day clock
2. Set OS-9 clock from hardware clock
3. Read/write all I/O registers internal to the MC 68360
4. Get/Set all programmable controls on serial ports
5. Verify that the 120 Hz interrupt is functioning
6. Set, configure, and read timers
7. Observe time-out interrupts

9.2.7.6.5 The OS-9 Shell Utility shall communicate with the user through the SP4 Port. When invoked, a low-priority task shall be executed for each SP port 1 and 2. Each task shall be configurable to use a different combination of input buffering options. The task shall open the port, configure it, and then enter a processing loop. In the loop, it shall wait for input and echo any input to the output. If no input is received for one second, an ASCII text string shall be sent out on the port. This text string shall be of the form “port P hh:mm:ss.” P is the port number and hh:mm:ss is the current OS-9 time stamp. The text shall be terminated with a carriage return followed by a line feed character.

9.2.7.6.6 Source and object Software shall be provided to the QPL or Purchasing AGENCY on both document listing and CD Memory. It shall provide user descriptions of test logic and reports. The AGENCY shall possess non- exclusive rights to this program suite.

9.2.7.7 DELIVERABLES

9.2.7.7.1 A software package resident on the FLASH Memory shall be provided, including the Embedded OS-9 kernels, platform drivers, and a validation suite.

9.2.7.7.2 All software shall be delivered in the following forms:

1. Fully commented source code of contractor developed software (OS-9 not required)

2. Microware Ultra-C Version 1.1 compatible linkable object code
3. Memory map listing

9.2.7.7.3 Specific hardware memory addresses shall be specified and provided in a supplied INCLUDE FILE as defined constants. The INCLUDE FILE shall meet all applicable software delivery requirements.

9.2.7.7.4 Timer usage by drivers and their uninterrupted execution latencies, error values returned by driver calls, error codes, and a format of the error report file shall be documented.

9.2.7.7.5 Software to initialize and perform a power-up self-test of the CPU Module prior to the initialization of the OS-9 operating system shall be provided. All software components detailed in this specification or otherwise, and requiring initialization, shall be identified and the required initialization and nature of the test, documented. In addition, software provided to perform initialization and/or test shall be documented.

9.2.7.7.6 OS-9 compliant header files shall be provided with all Driver Modules.

Section 3 MODEL 2070-2 FIELD I/O MODULE (FI/O)

9.3.1 The MODEL 2070-2A MODULE shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

9.3.2 The MODEL 2070-2B MODULE shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

9.3.3 FIELD CONTROLLER UNIT (FCU): The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware.

9.3.4 PARALLEL I/O PORTS: The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

9.3.4.1 The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 Megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

9.3.4.2 Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

9.3.5 **OTHER MODULE CIRCUIT FUNCTIONS**

9.3.5.1 A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

9.3.5.2 An External WDT “Muzzle” Jumper shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 ms for 3.5 seconds or due to CPU Command. When the jumper is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.3.5.3 A WATCHDOG Circuit shall be provided. It shall be enabled by the FIELD I/O software at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

9.3.5.4 ONE KHz REFERENCE: A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

9.3.5.5 A 32-bit MILLISECOND COUNTER (MC) shall be provided for “timestamping.” Each 1 KHz reference interrupt shall increment the MC.

9.3.5.6 At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the “E” Bit and a subsequent set output command is processed.

9.3.5.7 A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of

SP3. An LED shall be provided on the module front panel labeled “SP3 ON”. If LED is ON, SP3 is active and available at C12S.

9.3.6 **SERIAL COMMUNICATIONS / LOGIC CIRCUITRY**

9.3.6.1 System Serial Port 5 (SP5)) EIA 485 signal Lines shall enter the I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

9.3.6.2 System Serial Port 3 (SP3) EIA 485 signal lines shall enter the I/O module and be isolated, converted back to EIA 485 and then routed to Connector C12S.

9.3.6.3 LINESYNC and POWER DOWN Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

9.3.6.4 CPU RESET and POWER UP (SYSRESET) Lines shall be isolated and “OR’d” to form NRESET. NRESET shall be used to reset FCU and other module devices. NRESET shall also, be converted to EIA 485, then routed to Connector C12S.

9.3.6.5 If the module is 2070-2B, routing to FCU doesn’t apply.

9.3.6.6 Isolation is between internal +5DC / DCG#1 and +12 DC ISO/DCG#2. +12 DC ISO shall be used for board power and external logic.

9.3.7 **BUFFERS:** A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry			
Description	msb	lsb	Byte Number
Transition Entry Identifier	S Input Number		1
Timestamp NLSB	x x x x x x x x		2
Timestamp LSB	x x x x x x x x		3

Figure 9-17: TRANSITION BUFFER, INPUT TRANSITION ENTRY

Millisecond Counter Rollover Entry			
Description	msb	lsb	Byte Number
Rollover Entry Identifier	1 1 1 1 1 1 1 1		1
Timestamp MSB	x x x x x x x x		2
Timestamp NMSB	x x x x x x x x		3

Figure 9-18: TRANSITION BUFFER, ROLLOVER ENTRY

9.3.8 **I/O FUNCTIONS**

9.3.8.1 INPUTS

9.3.8.1.1 Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb.

9.3.8.1.2 Each complete input scan shall finish within 100 μs. Once sampled, the Logic State of input shall be held until the next input scan.

9.3.8.1.3 Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 μs.

9.3.8.1.4 If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer.

9.3.8.1.5 If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 μs of the completion of the input scan.

9.3.8.2 DATA FILTERING

9.3.8.2.1 If configured, the inputs shall be filtered by the FCU to remove signal bounce.

9.3.8.2.2 The filtered input signals shall then be monitored for changes as noted.

9.3.8.2.3 The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples.

9.3.8.2.4 If the Ignore Input flag is set, no input transitions shall be recorded.

9.3.8.2.5 The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized.

9.3.8.2.6 If the change of state is shorter than the specified value, the change of state shall be ignored.

9.3.8.2.7 The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering Enabled.
On and off filter values shall be set to 5.
Transition monitoring Disabled (Timestamps are not logged).

Figure 9-19: DEFAULT FILTERING VALUES

9.3.8.3 OUTPUTS

9.3.8.3.1 Simultaneous assertion of all outputs shall occur within 100 μs.

9.3.8.3.2 Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC.

9.3.8.3.3 The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module.

9.3.8.3.4 If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

9.3.8.4 Standard Function: Each output shall be controlled by the data and control bits in the CPU Module-FI/O frame protocol as follows:

9.3.8.4.1 Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function:
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

Figure 9-20: OUTPUT BIT TRANSLATION

9.3.8.4.2 In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured.

9.3.8.4.3 For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle.

9.3.8.4.4 In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch nor change state unless configured to do so.

9.3.8.5 INTERRUPTS

9.3.8.5.1 All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts.

9.3.8.5.2 MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command.

9.3.8.5.3 LINESYNC Interrupt: This interrupt shall be generated by both the 0- 1 and 1-0 transitions of the LINESYNC signal.

9.3.8.5.3.1 The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($60 consecutive LINESYNC interrupts).

9.3.8.5.3.2 The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second.

9.3.8.5.3.3 A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($500 consecutive millisecond interrupts).

9.3.8.6 Communication Service Routine: A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

9.3.8.6.1 For Transmission:

- Generate the opening and closing flags.
- Generate the CRC value.
- Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU.
- Provide zero bit insertion.

9.3.8.6.2 For Receiving:

- Detect the opening and closing flags.
- Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module.
- Strip out inserted zeros.
- Calculate the CRC value, compare it to the received value, and generate an interrupt on an error.
- Generate an interrupt if an abort sequence is received.

9.3.8.7 Communication Processing: The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

9.3.8.8 Input Processing: This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9.3.9 **DATA COMMUNICATION PROTOCOLS**

9.3.9.1 Protocols: All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.

9.3.9.1.1 The frame type shall be determined by the value of the first byte of the message. The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types				
Module Command	I/0 Module Response	Description:	Minimum Message Time	Maximum Message Time
49	177	Request Module Status	250 μs	275 us
50	178	MILLISECOND CTR. Mgmt.	222.5 μs	237.5 us
51	179	Configure Inputs	344.5 μs	6.8750 ms
52	180	Poll Raw Input Data	317.5 μs	320 μs
53	181	Poll Filtered Input Data	317.5 μs	320 μs
54	182	Poll Input Transition Buffer	300 μs	10.25 ms
55	183	Command Outputs	405 μs	410 μs
56	184	Config. Input Tracking Functions	340 μs	10.25 ms
57	185	Config. Complex Output Functions	340 μs	6.875 ms
58	186	Configure Watchdog	222.5 μs	222.5 μs
59	187	Controller Identification	222.5 μs	222.5 μs
60	188	I/O Module Identification	222.5 μs	222.5 μs
61-62	189-190	Reserved (note below)		
63	191	Poll variable length raw input	317.5 μs	320 μs
64	192	Variable length command outputs	405 μs	410 μs

Figure 9-21: 2070 SDLC FRAME TYPES

9.3.9.1.2 Message's 61 / 189 and 62 / 190 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (pending TEES Chapter 7).

9.3.9.1.3 Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of input bytes.

9.3.9.1.4 Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes along with the following output data.

9.3.9.2 REQUEST MODULE STATUS: The Command shall be used to request FI/O status information response. Command/response frames are as follows:

9.3.9.2.1 Request Module Status Command

REQUEST MODULE STATUS COMMAND									
Description	msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Figure 9-22: REQUEST MODULE STATUS COMMAND

9.3.9.2.2 Request Module Status Response

Request Module Status Response									
Description	msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

Figure 9-23: REQUEST MODULE STATUS RESPONSE

9.3.9.2.3 The response status bits are defined as follows:

P	Indicates FI/O hardware reset
E	Indicates a communications loss of greater than 2 seconds
M	Indicates an error with the MC interrupt
L	Indicates an error in the LINESYNC
W	Indicates that the FI/O has been reset by the Watchdog
R	Indicates that the EIA-485 receive error count byte has rolled over
T	Indicates that the EIA-485 transmit error count byte has rolled over
K	Indicates the Datakey has failed or is not present

Figure 9-24: RESPONSE STATUS BITS

9.3.9.2.4 Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.

9.3.9.3 MC MANAGEMENT frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

9.3.9.3.1 MILLISECOND COUNTER MANAGEMENT COMMAND:

Millisecond Counter Management Command									
Description	msb							lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	X	x	X	x	x	x	x	Byte 2
New Timestamp NMSB	x	X	x	X	x	x	x	x	Byte 3
New Timestamp NLSB	x	X	x	X	x	x	x	x	Byte 4
New Timestamp LSB	x	X	x	X	x	x	x	x	Byte 5

Figure 9-25: MILLISECOND COUNTER MANAGEMENT COMMAND

9.3.9.3.2 MILLISECOND COUNTER MANAGEMENT RESPONSE:

Millisecond Counter Management Response									
Description	msb							Lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Figure 9-26: Millisecond Counter Management Response

9.3.9.4 CONFIGURE INPUTS: The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

9.3.9.4.1 CONFIGURE INPUTS COMMAND:

Configure Inputs Command									
Description	msb				lsb				Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	N	n	N	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Figure 9-27: Configure Inputs Command

9.3.9.4.2 CONFIGURE INPUTS RESPONSE:

Configure Inputs Response									
Description	msb				lsb				Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Figure 9-28: Configure Inputs Response

9.3.9.4.3 Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input
e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)
r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)
S - return status S = '0' on completion or '1' on error

Figure 9-1 Block field definitions

9.3.9.5 POLL RAW INPUT DATA: The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 or 15 bytes of information indicating the current input status. The frames are as follows:

9.3.9.5.1 POLL RAW INPUT DATA COMMAND:

Poll Raw Input Data Command									
Description	msb				lsb				Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Figure 9-29: POLL RAW INPUT DATA COMMAND

9.3.9.5.2 POLL RAW INPUT DATA RESPONSE:

Poll Raw Input Data Response									
Description	msb				lsb				Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

Figure 9-30: POLL RAW INPUT DATA RESPONSE

9.3.9.6 POLL FILTERED INPUT DATA: The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes(-2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

9.3.9.6.1 POLL FILTER INPUT DATA COMMAND:

Poll Filter Input Data Command									
Description	msb							lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Figure 9-31: POLL FILTER INPUT DATA COMMAND

9.3.9.6.2 POLL FILTER INPUT DATA RESPONSE:

Poll Filter Input Data Response									
Description	msb							lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

Figure 9-32: POLL FILTER INPUT DATA RESPONSE

9.3.9.7 POLL INPUT TRANSITION BUFFER: The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

9.3.9.7.1 POLL INPUT TRANSITION BUFFER COMMAND:

Poll Input Transition Buffer Command									
Description	msb				lsb				Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2

Figure 9-33: POLL INPUT TRANSITION BUFFER COMMAND

9.3.9.7.2 INPUT TRANSITION BUFFER RESPONSE:

Input Transition Buffer Response									
Description	msb				lsb				Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2
Number of Entries	x	x	x	X	x	X	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
Timestamp MSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+8
Timestamp NMSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+9
Timestamp NLSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+10
Timestamp LSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+11

Figure 9-34: INPUT TRANSITION BUFFER RESPONSE

9.3.9.7.3 Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

S - Indicates the state of the input after the transition
C - Indicates the 255 entry buffer limit has been exceeded
F - Indicates the 1024 buffer limit has been exceeded
G - Indicates the requested block number is out of monotonic increment sequence
E - Same block number requested, E is set in response

9.3.9.7.4 The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

9.3.9.8 SET OUTPUTS: The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

9.3.9.8.1 SET OUTPUTS COMMAND:

Set Outputs Command									
Description	msb				lsb				Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	X	x	x	X	x	x	x	x	Byte 2
Outputs O8 to O103 Data	X	x	x	X	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	X	x	x	X	x	x	x	x	Byte 15
Outputs O8 to O103 Control	X	x	x	X	x	x	x	x	Bytes 16 to 27

Figure 9-35: SET OUTPUTS COMMAND

9.3.9.8.2 SET OUTPUTS RESPONSE:

Set Outputs Response									
Description	msb				lsb				Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

Figure 9-36: SET OUTPUTS RESPONSE

9.3.9.9 CONFIGURE INPUT-TRACKING FUNCTIONS: The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to ‘1’ and the command shall not be implemented. The command and response frames are as follows:

9.3.9.9.1 CONFIGURE INPUT TRACKING FUNCTIONS COMMAND:

Configure Input Tracking Functions Command									
Description	msb				lsb				Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Figure 9-37: CONFIGURE INPUT TRACKING FUNCTIONS COMMAND

9.3.9.9.2 CONFIGURE INPUT TRACKING FUNCTIONS RESPONSE:

Configure Input Tracking Functions Response									
Description	msb				lsb				Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	X	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	X	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	X	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	X	x	x	x	x	Byte 6

Figure 9-38: CONFIGURE INPUT TRACKING FUNCTIONS RESPONSE

9.3.9.9.3 Definitions are as follows:

E	'1' -	Enable input tracking functions for this output
	'0' -	Disable input tracking functions for this output
I	'1' -	The output is OFF when input is ON, ON when input OFF
	'0' -	The output is ON when input is ON, OFF when input is OFF
V	'1' -	The max. number of 8 configurable outputs has been exceeded
	'0' -	No error

9.3.9.9.3.1 Number of Items: The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

9.3.9.9.4 The timestamp value shall be sampled prior to the response frame.

9.3.9.9.5 Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

9.3.9.9.6 The “Number of Item” field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message “V” bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

9.3.9.10 CONFIGURE COMPLEX OUTPUT FUNCTIONS: The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

9.3.9.10.1 CONFIGURE COMPLEX OUTPUT FUNCTIONS COMMAND:

Configure Complex Output Functions Command									
Description	msb							lsb	Byte Number
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Figure 9-39: CONFIGURE COMPLEX OUTPUT FUNCTIONS COMMAND

9.3.9.10.2 CONFIGURE COMPLEX OUTPUT FUNCTIONS RESPONSE:

Configure Complex Output Functions Response									
Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	X	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	X	X	x	x	x	Byte 4
Timestamp (NLSB)	x	X	x	X	X	x	x	x	Byte 5
Timestamp (LSB)	x	X	x	X	X	x	x	x	Byte 6

Figure 9-40: CONFIGURE COMPLEX OUTPUT FUNCTIONS RESPONSE

9.3.9.10.3 The bit fields of the command frame are defined as follows:

E	'1'	Enable complex output function for this output.
	'0'	Disable complex output function for this output.
J	'1'	During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
	'0'	During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.
Output Number:		7-bit output number identifying outputs
Primary Duration:		For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.
Secondary Duration:		For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.
F	'1'	The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
	'0'	The trigger or gate shall be derived from the raw input.
R	'1'	For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
	'0'	For triggered output, the output shall be triggered by an OFF- to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
Input Number:		7-bit input number identifying inputs 0 Up.
P	'1'	The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
	'0'	The output is configured for continuous oscillation.
W	'1'	It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
	'0'	Operation shall begin within 2 ms of the command receipt.
G	'1'	Operation shall be gated active by the specified input.
	'0'	Gating is inactive.
L	'1'	The LINESYNC based clock shall be used for the time ticks.
	'0'	The MC shall be used for the time ticks.
V	'1'	Indicates maximum number of configurable outputs is exceeded.
	'0'	No error
Number of items:		The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

Figure 9-41: The bit fields of the command frame

9.3.9.10.4 Controlling input signals shall be sampled at least once per millisecond.

9.3.9.10.5 The “Number of Items” field is valid from 0 to 16.

9.3.9.10.5.1 Zero means disable all Complex Output functions.

9.3.9.10.5.2 Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables.

9.3.9.10.5.3 If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message “V” bit shall be set to 1.

9.3.9.10.5.4 If an invalid output or input number (the “G” or “W” bits being set to 1) is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed.

9.3.9.10.5.5 When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command.

9.3.9.10.5.6 When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it.

9.3.9.10.5.7 The “G” bit (gating) set to 1 takes precedence over the “W” bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the “W” bit in the command message.

9.3.9.10.5.8 If a Complex Output is configured with the “G” bit set to 1 (gating) and the “P” bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive).

9.3.9.10.5.9 For a single pulse operation (“G” bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

9.3.9.11 CONFIGURE WATCHDOG: The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

9.3.9.11.1 CONFIGURE WATCHDOG COMMAND:

Configure Watchdog Command									
Description	msb				lsb				Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	X	x	x	x	x	Byte 2

Figure 9-42: CONFIGURE WATCHDOG COMMAND

9.3.9.11.2 CONFIGURE WATCHDOG RESPONSE:

Configure Watchdog Response									
Description	msb				lsb				Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

Figure 9-43: CONFIGURE WATCHDOG RESPONSE

9.3.9.11.3 The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

9.3.9.11.4 On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

9.3.9.12 CONTROLLER IDENTIFICATION: This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit “K” shall be set and no interrogation shall take place. If a error occurs during the interrogation, Bit “K” shall be set. If “K” bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

9.3.9.12.1 CONTROLLER IDENTIFICATION COMMAND:

Controller Identification Command									
Description	msb				lsb				Byte Number
Type Number= 59	0	0	1	1	1	0	1	1	Byte 1

Figure 9-44: CONTROLLER IDENTIFICATION COMMAND

9.3.9.12.2 CONTROLLER IDENTIFICATION RESPONSE:

Controller Identification Response									
Description	msb				lsb				Byte Number
Type Number = 187	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Bytes 3 to 130

Figure 9-45: CONTROLLER IDENTIFICATION RESPONSE

9.3.9.13 MODULE IDENTIFICATION: The FI/O Identification command frame shall be used to request the FI/O Identification value Response of "1" for the 2070-2A, "2" for the 2070-8 FI/O, and "32 to 40" for ITS Cabinet SIUs and SMU/TMU. The command and response frames are shown as follows:

9.3.9.13.1 I/O MODULE IDENTIFICATION COMMAND:

I/O Module Identification Command									
Description	msb				lsb				Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

Figure 9-46: I/O MODULE IDENTIFICATION COMMAND

9.3.9.13.2 I/O MODULE IDENTIFICATION RESPONSE:

I/O Module Identification Response									
Description	msb				lsb				Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
FI/O I D byte	x	x	x	X	x	x	x	x	Byte 2

Figure 9-47: I/O MODULE IDENTIFICATION RESPONSE

Section 4 MODEL 2070-3 FRONT PANEL ASSEMBLY (FPA)

9.4.1 The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU active LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A: FPA controller, two keyboards, AUX (Stop Time) switch, alarm bell & Display A
OPTION 3B: FPA controller, two keyboards, AUX (Stop Time) switch, alarm bell & Display B
OPTION 3C: System Serial Port 6 Lines, isolated and vectored to Connector C60S.

9.4.2 Two KEYBOARDS shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

9.4.3 The cathode of the CPU ACTIVE LED INDICATOR shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.

9.4.4 The DISPLAY shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with a minimum character dimensions of 5.00 mm wide by 10.44 mm high and an electro -luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 2.65 mm wide by 4.24 mm high and either LED or EL backlight.

9.4.4.1 Each character shall be composed of a 5 x 7 dot matrix with a underline row or a 5 x 8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90°) viewing, +/-35° vertical, +/-45° horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

9.4.4.2 The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

9.4.4.3 Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

9.4.5 **The FPA CONTROLLER** shall function as the Front Panel Device controller interfacing with the CPU Module.

9.4.5.1 A FPA RESET Switch shall be provided on the Assembly PCBA. The momentary CONTROL switch shall be logic OR'd with the CPU RESET Line, producing a FPA RESET Output. Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following shall occur:

1. Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
2. Each special character shall be set to ASCII SPC (space).
3. The tab stops shall be set to columns 9, 17, 25, and 33.
4. The backlight timeout value shall be set to 6 (60 seconds).
5. The backlight shall be extinguished.
6. The display shall be cleared (all ASCII SPC).
7. The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is " ESC [PU", hex value "1B 5B 50 55".

9.4.5.2 When a key-press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

9.4.5.3 Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

9.4.5.4 When the AUX (Stop Time) Switch is toggled, the appropriate AUX (Stop Time) Switch code shall be transmitted to the CPU.

9.4.5.5 The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User composed characters shall be represented in the communication protocol on Page 9-7-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

9.4.5.6 Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

9.4.5.7 Auto-wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

9.4.5.8 Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

9.4.5.9 Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60 % ON / 40 % OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

9.4.5.10 Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

9.4.5.11 Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

9.4.5.12 Displayable characters shall be refreshed at least 20 times per second.

9.4.5.13 The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

9.4.5.14 The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows	
Pn:	Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.
P1:	Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)
Px:	Display column number (1-40), using one ASCII character per digit without leading zero.
Py:	Display line (1-4) one ASCII character
Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).	
...	Continue the list in the same fashion:
2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.	
3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).	

Figure 9-48: The Front Panel Assembly Command Codes conventions

9.4.5.15 The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

9.4.5.16 C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

9.4.6 The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

Section 5 MODEL 2070-4 POWER SUPPLY MODULE

9.5.1 The Model 2070-4 Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices. The Model 2070-4B Module shall meet the same requirements as the 2070-4A except for 3.5 Amperes of +5 VDC and the +5 VDC STANDBY Power.

9.5.2 An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

9.5.3 INPUT PROTECTION: Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

9.5.4 +5 VDC STANDBY POWER shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 to +2 VDC for over 600 minutes.

9.5.5 MONITOR CIRCUITRY shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

9.5.5.1 The ACFAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately upon Power Failure. The Lines shall transition to HIGH at Power Restoration. The Lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/-25 ms after ACFAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 +/- 25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

9.5.5.2 The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

9.5.5.3 The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ±1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

9.5.5.4 The LINESYNC shall continue until SYSRESET transitions LOW and begin then SYSRESET transitions HIGH.

9.5.6 **POWER SUPPLY REQUIREMENTS**

Voltage	Tolerances	I Minimum	I Maximum
+5 VDC	+4.875 to +5.125 VDC	1.0 AMP	10.0 AMP: MODULE 2070-4A 3.5 AMP – MODULE 2070-4B
+12 VDC Serial	+11.4 to +12.6 VDC	0.1 AMP	0.5 AMP
12 VDC Serial	-11.4 to –12.6 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11.4 to +12.6 VDC	0.1 AMP	1.0 AMP

Figure 9-49: POWER SUPPLY REQUIREMENTS

9.5.6.1 Line/Load Regulation: shall meet the table tolerances values for voltage range of 90 to 135 VAC, minimum and maximum loads called out in the table & including ripple noise.

9.5.6.2 Efficiency: 70 % minimum

9.5.6.3 Ripple & noise: Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater.

9.5.6.4 Voltage Overshoot: No greater than 5 %, all outputs.

9.5.6.5 Over voltage Protection: 130% Vout for all outputs.

9.5.6.6 Overload & Short: Power fold back point 120% of max rated power Circuit Protection: Automatic recovery upon removal of fault.

9.5.6.7 Inrush Current: Cold Start Inrush shall be less than 25A at 115VAC.

9.5.6.8 Transient response: Output voltage back to within 1% in less than 500 μs on a 50% Load change. Peak transient not to exceed 5%.

9.5.6.9 Holdup Time: The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

9.5.6.10 Remote Sense: +5 VDC compensates 250 mV total line drop. Open sense load protection required.

Section 6 UNIT CHASSIS AND MODEL 2070-5 VME CAGE ASSEMBLY

9.6.1 **GENERAL:** The Chassis shall consist of the metal housing, Serial Motherboard, Backplane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.6.2 SERIAL MOTHERBOARD shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the MOTHERBOARD PCBA (provide strain relief). Test points shall be provided on the FPA side of the MOTHERBOARD for PS2 lines. A wiring harness FP shall be provided, linking the MOTHERBOARD with the FPA.

9.6.3 MODEL 2070-5 VME CAGE ASSEMBLY shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors shall be A24: D16 Interface.

9.6.4 The Model 2070–1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

Section 7 CHAPTER DETAILS

9.7.1 TEES Drawing 9-7-1,MODEL 2070 CHASSIS, FRONT VIEW

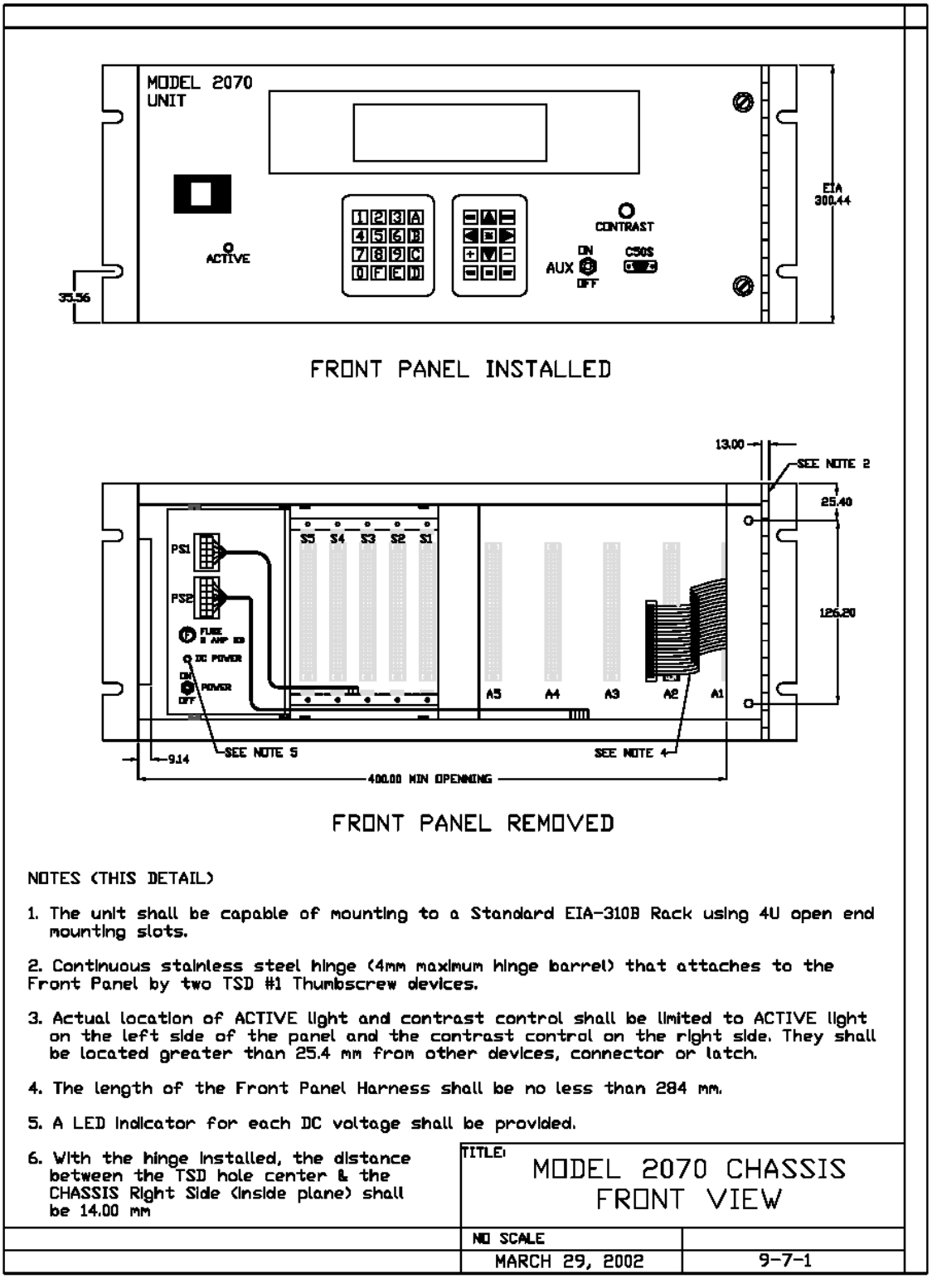


Figure 9-50: MODEL 2070 CHASSIS, FRONT VIEW, TEES

9.7.2 TEES 9-7-2, MODEL 2070 CHASSIS, REAR VIEW

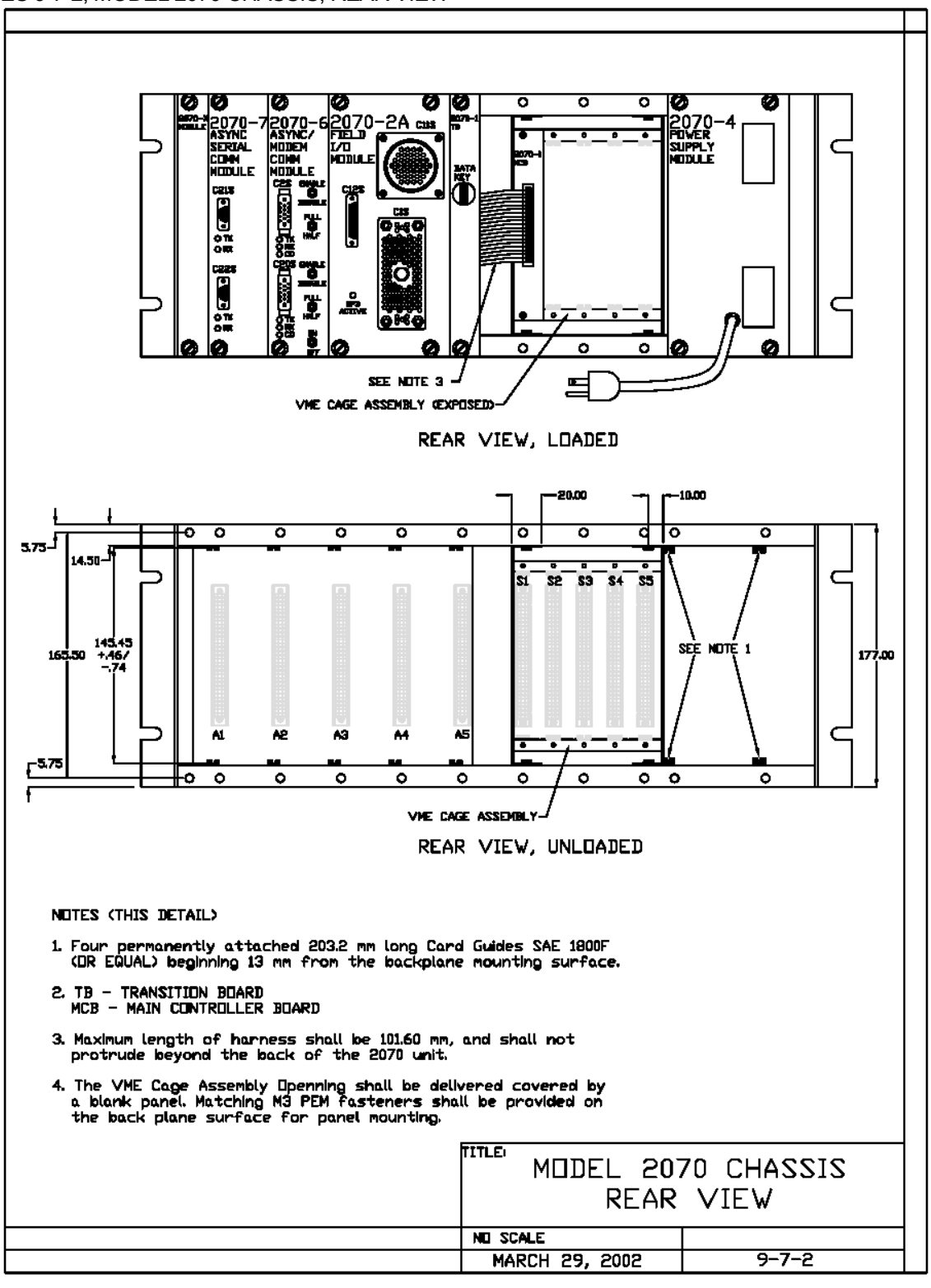


Figure 9-51: MODEL 2070 CHASSIS, REAR VIEW

9.7.3 TEES 9-7-3, MODEL 2070 CHASSIS, TOP VIEW

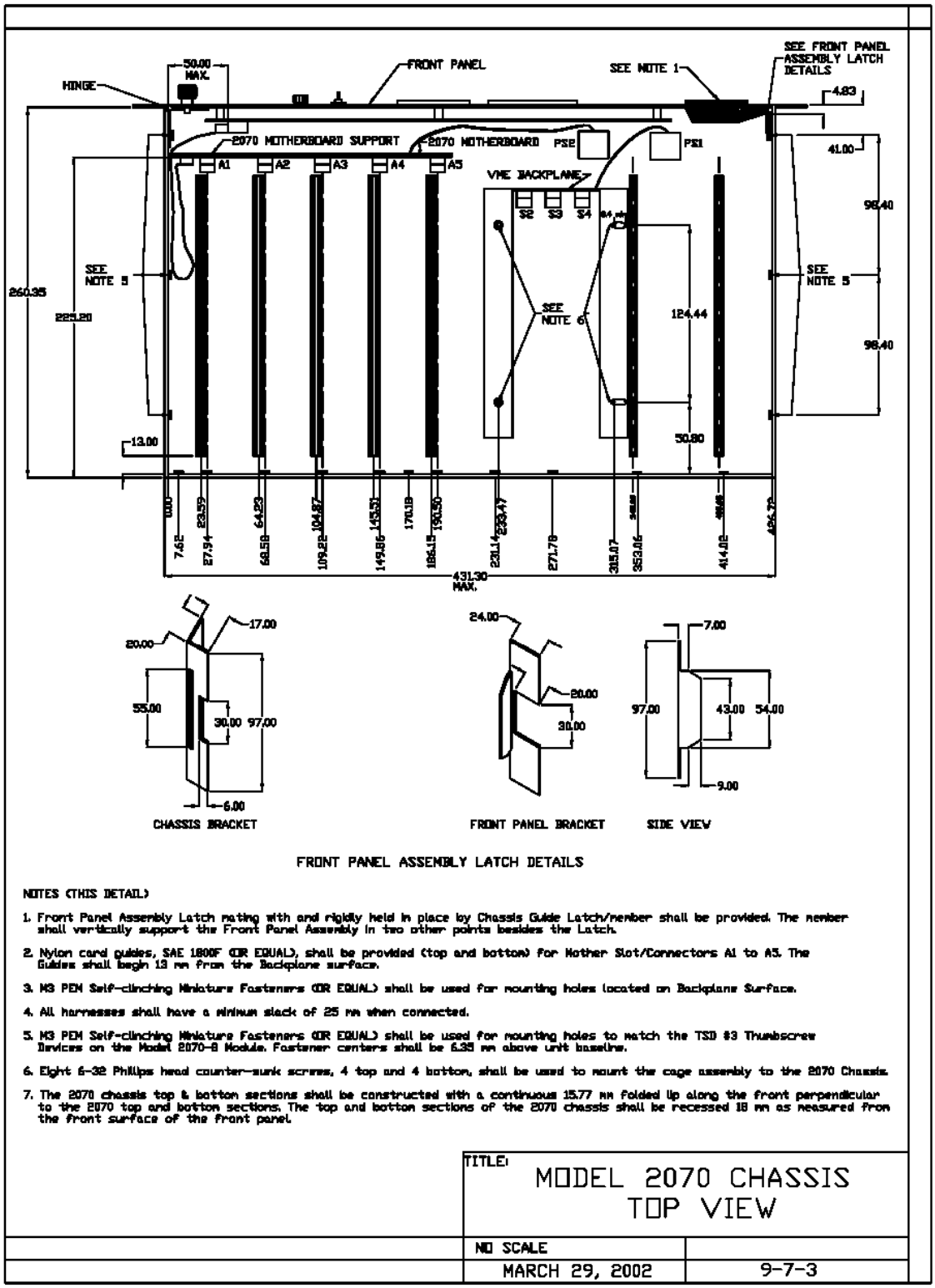
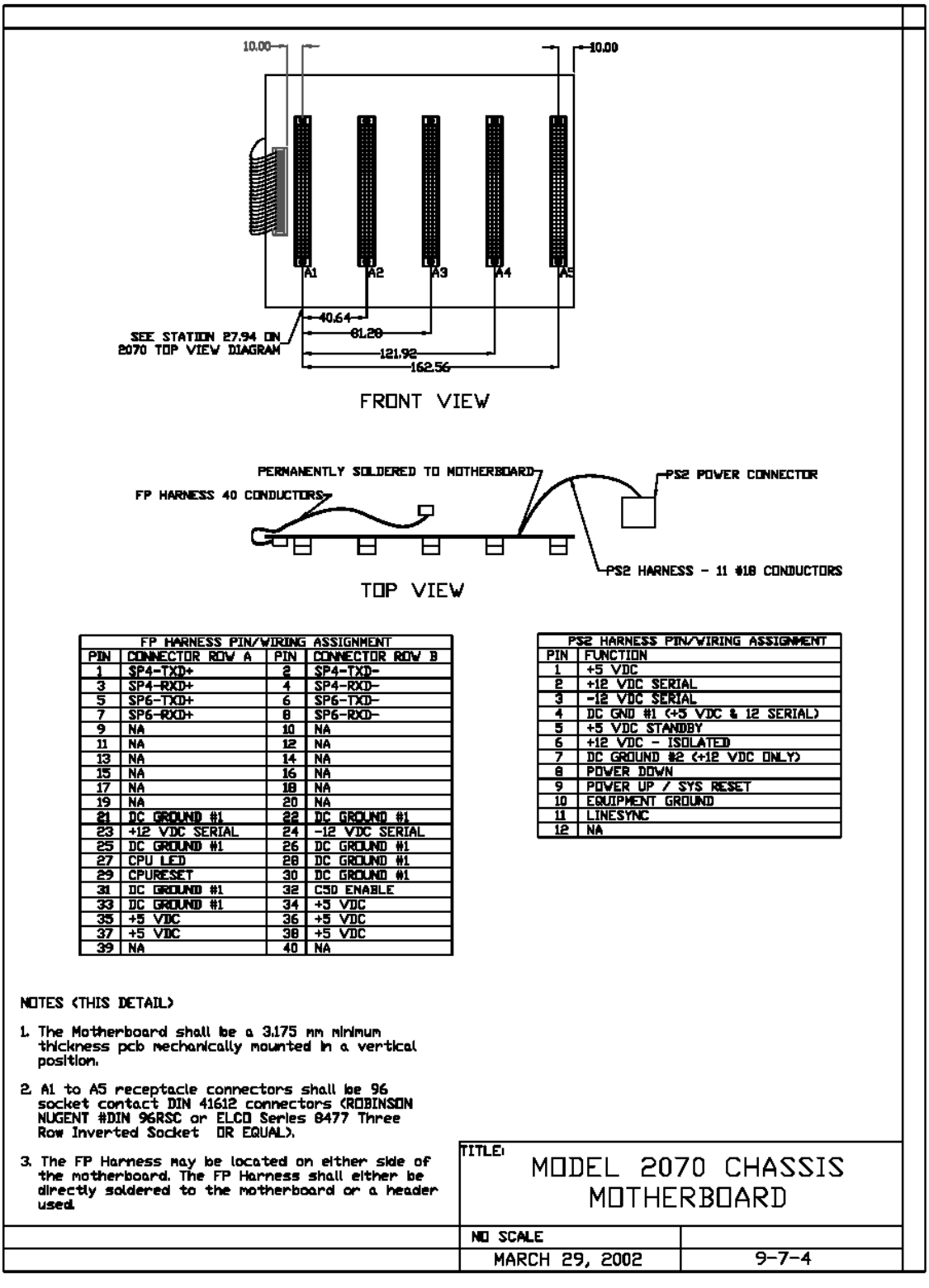


Figure 9-52: MODEL 2070 CHASSIS, TOP VIEW

9.7.4 TEES 9-7-4 MODEL 2070 CHASSIS, MOTHERBOARD



FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C5D ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.
2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).
3. The FP Harness may be located on either side of the motherboard. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE: MODEL 2070 CHASSIS MOTHERBOARD

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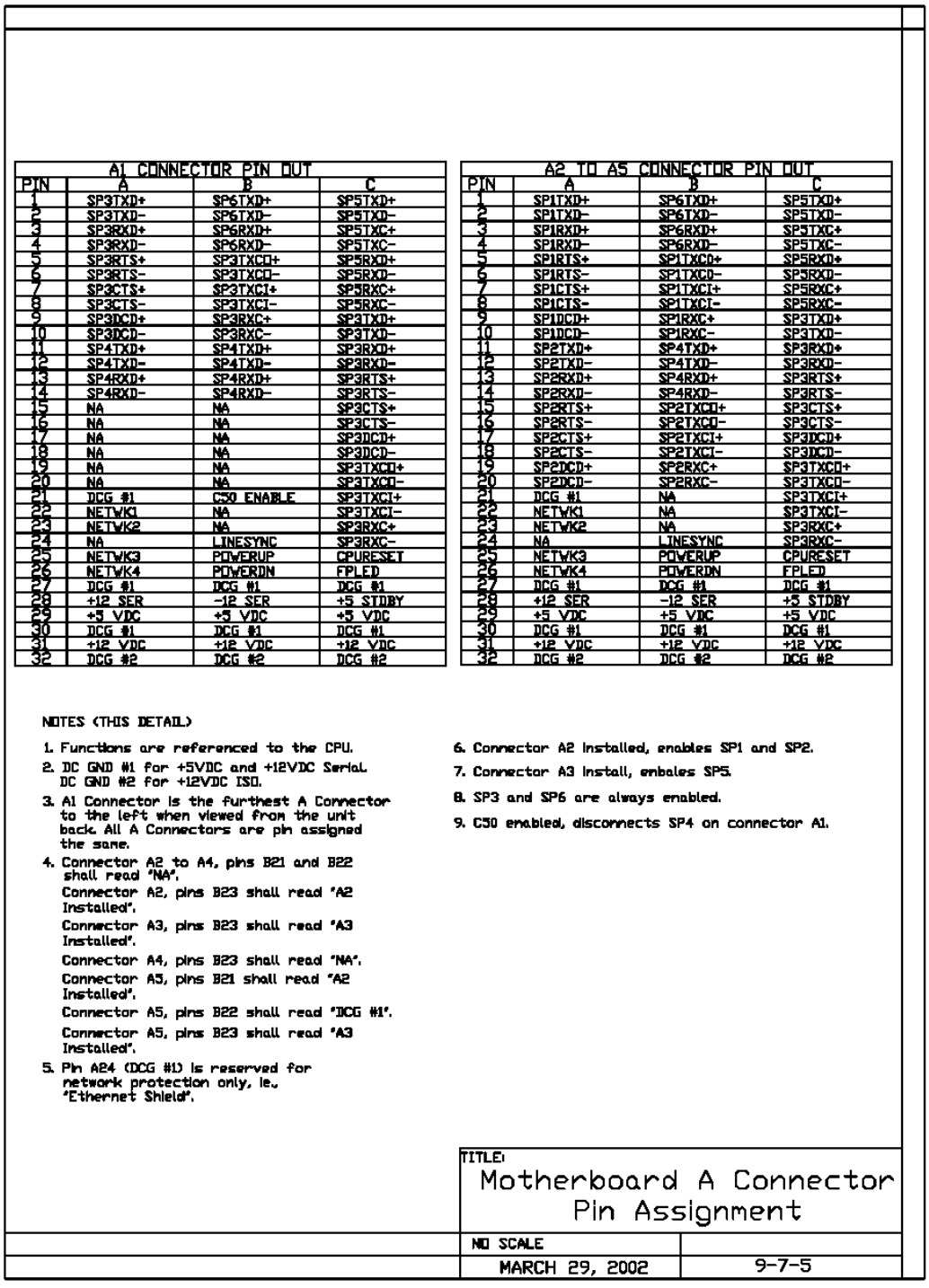
Figure 9-53: MODEL 2070 CHASSIS, MOTHERBOARD

9.7.5 TEES 9-7-5, note 4 addition: Signal pins SP1-TXD+, SP1-RXD+, SP1-RTS+, SP1-CTS+, SP1-DCD+, SP1-TXC(0)+, and SP1-RXC+ in the “A2”, “A3”, and “A4” connectors shall be assigned respectively to MC68360’s SCC1-TXD1, SCC1-RXD1,SCC1-RTS1, SCC1-CTS1, SCC1-CD1, SCC1-TCLK1, and SCC1-RCLK1, when SP1 of a model 2070 is used as an Ethernet port



A1 CONNECTOR PIN OUT

PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXCD+	SP5RXD+
6	SP3RTS-	SP3TXCD-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXCD+
20	NA	NA	SP3TXCD-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT

PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXCD+	SP5RXD+
6	SP1RTS-	SP1TXCD-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCD+	SP3CTS+
16	SP2RTS-	SP2TXCD-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCD+
20	SP2DCD-	SP2RXC-	SP3TXCD-
21	DCG #1	NA	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (DCG #1) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 install, enbales SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

TITLE:
Motherboard A Connector Pin Assignment

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9-7-5

Figure 9-54: MOTHERBOARD A CONNECTOR PIN ASSIGNMENT

9.7.6 TEES DRAWING 9-7-6, Type 2070 System PCB Modules, General

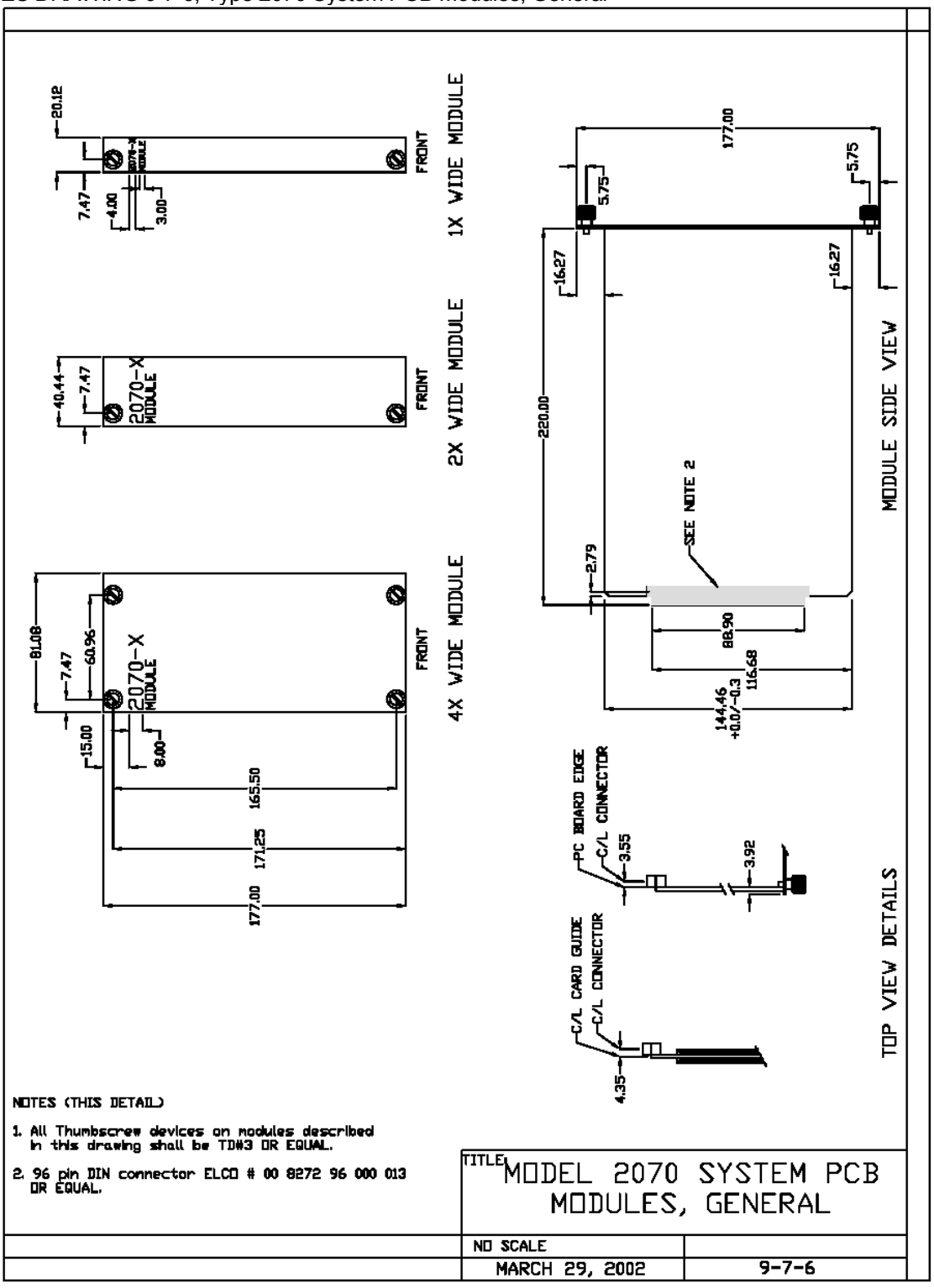


Figure 9-55: TEES DRAWING 9-7-6, Type 2070 System PCB Modules, General

9.7.7 TEES 9-7-7, MODEL 2070-1: CPU MODULE

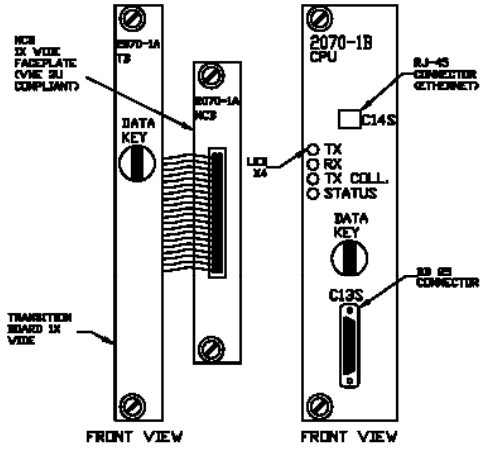
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT

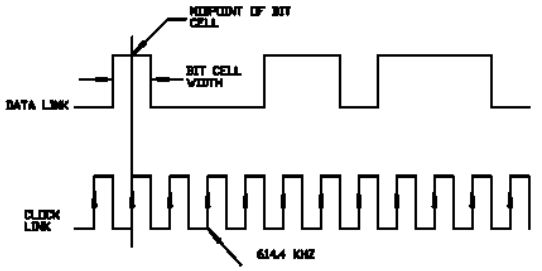
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1)	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC

SDLC FRAME LAYOUT

OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS + **	18	SP8 RTS - **
6	SP8 CTS + **	19	SP8 CTS - **
7	SP8 DCD + **	20	SP8 DCD - **
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

C14S PIN ASSIGNMENT (ETHERNET)

PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4
2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6
3. * Default BPS Rate for Indicated Port.
   ** Disconnected by internal switch.
4. SP1 OF THE 2070-1A Is 68360 SCC1. SP1 OF THE 2070-1B Is Dual SCC1 with 68360 SCC1 assigned to ETHERNET.
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

TITLE: MODEL 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL

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Figure 9-56: Type 2070-1 CPU Modules and Serial Port/SDLC Protocol

9.7.8 TEES DRAWING 9-7-8, Type 2070-2 Field I/O Modules

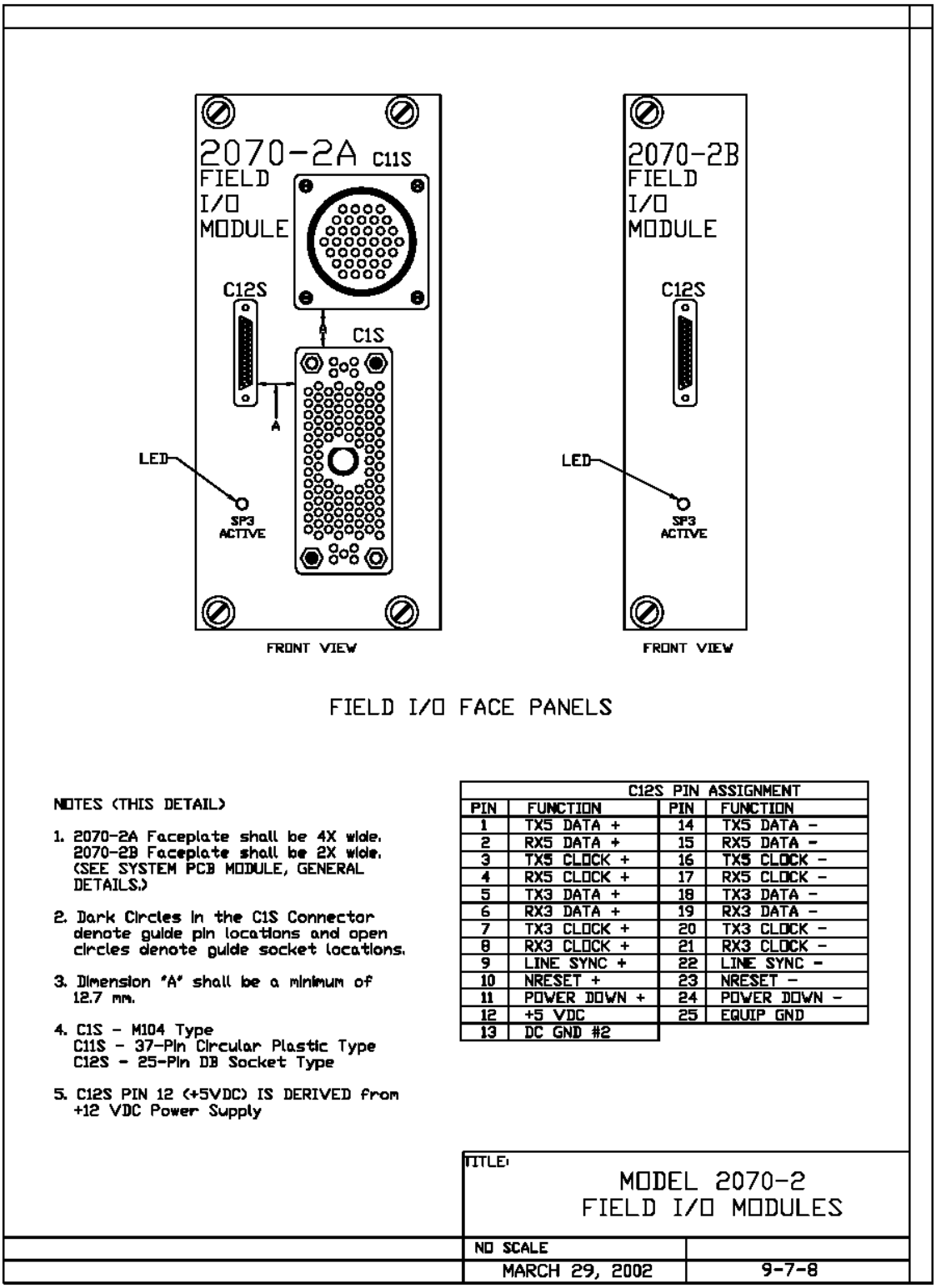


Figure 9-57: TEES DRAWING 9-7-8, Type 2070-2 Field I/O Modules

9.7.9 TEES DRAWING 9-7-9, Type 2070-2A Field I/O Module C1 & C11 Connectors

C1S PIN ASSIGNMENT

PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION	
	NAME	PORT		NAME	PORT		NAME	PORT		NAME	PORT
1	DC GROUND		27	O24	O4-1	53	I14	I2-7	79	I44	I6-5
2	O0	O1-1	28	O25	O4-2	54	I15	I2-8	80	I45	I6-6
3	O1	O1-2	29	O26	O4-3	55	I16	I3-1	81	I46	I6-7
4	O2	O1-3	30	O27	O4-4	56	I17	I3-2	82	I47	I6-8
5	O3	O1-4	31	O28	O4-5	57	I18	I3-3	83	O40	O6-1
6	O4	O1-5	32	O29	O4-6	58	I19	I3-4	84	O41	O6-2
7	O5	O1-6	33	O30	O4-7	59	I20	I3-5	85	O42	O6-3
8	O6	O1-7	34	O31	O4-8	60	I21	I3-6	86	O43	O6-4
9	O7	O1-8	35	O32	O5-1	61	I22	I3-7	87	O44	O6-5
10	O8	O2-1	36	O33	O5-2	62	I23	I3-8	88	O45	O6-6
11	O9	O2-2	37	O34	O5-3	63	I28	I4-5	89	O46	O6-7
12	O10	O2-3	38	O35	O5-4	64	I29	I4-6	90	O47	O6-8
13	O11	O2-4	39	I0	I1-1	65	I30	I4-7	91	O48	O7-1
14	DC GROUND		40	I1	I1-2	66	I31	I4-8	92	DC GROUND	
15	O12	O2-5	41	I2	I1-3	67	I32	I5-1	93	O49	O7-2
16	O13	O2-6	42	I3	I1-4	68	I33	I5-2	94	O50	O7-3
17	O14	O2-7	43	I4	I1-5	69	I34	I5-3	95	O51	O7-4
18	O15	O2-8	44	I5	I1-6	70	I35	I5-4	96	O52	O7-5
19	O16	O3-1	45	I6	I1-7	71	I36	I5-5	97	O53	O7-6
20	O17	O3-2	46	I7	I1-8	72	I37	I5-6	98	O54	O7-7
21	O18	O3-3	47	I8	I2-1	73	I38	I5-7	99	O55	O7-8
22	O19	O3-4	48	I9	I2-2	74	I39	I5-8	100	O36	O5-5
23	O20	O3-5	49	I10	I2-3	75	I40	I6-1	101	O37	O5-6
24	O21	O3-6	50	I11	I2-4	76	I41	I6-2	102	O38 DET RES	O5-7
25	O22	O3-7	51	I12	I2-5	77	I42	I6-3	103	O39 WDT	O5-8
26	O23	O3-8	52	I13	I2-6	78	I43	I6-4	104	DC GROUND	

C11S PIN ASSIGNMENT

PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION	
	NAME	PORT		NAME	PORT		NAME	PORT		NAME	PORT
1	O56	O8-1	11	I25	I4-2	21	I54	I7-7	31	DC GROUND	
2	O57	O8-2	12	I26	I4-3	22	I55	I7-8	32	NA	- - -
3	O58	O8-3	13	I27	I4-4	23	I56	I8-1	33	NA	- - -
4	O59	O8-4	14	DC GROUND		24	I57	I8-2	34	NA	- - -
5	O60	O8-5	15	I48	I7-1	25	I58	I8-3	35	NA	- - -
6	O61	O8-6	16	I49	I7-2	26	I59	I8-4	36	NA	- - -
7	O62	O8-7	17	I50	I7-3	27	I60	I8-5	37	DC GROUND	
8	O63	O8-8	18	I51	I7-4	28	I61	I8-6			
9	DC GROUND		19	I52	I7-5	29	I62	I8-7			
10	I24	I4-1	20	I53	I7-6	30	I63	I8-8			

TITLE: MODEL 2070-2A FIELD I/O MODULE C1 & C11 CONNECTORS

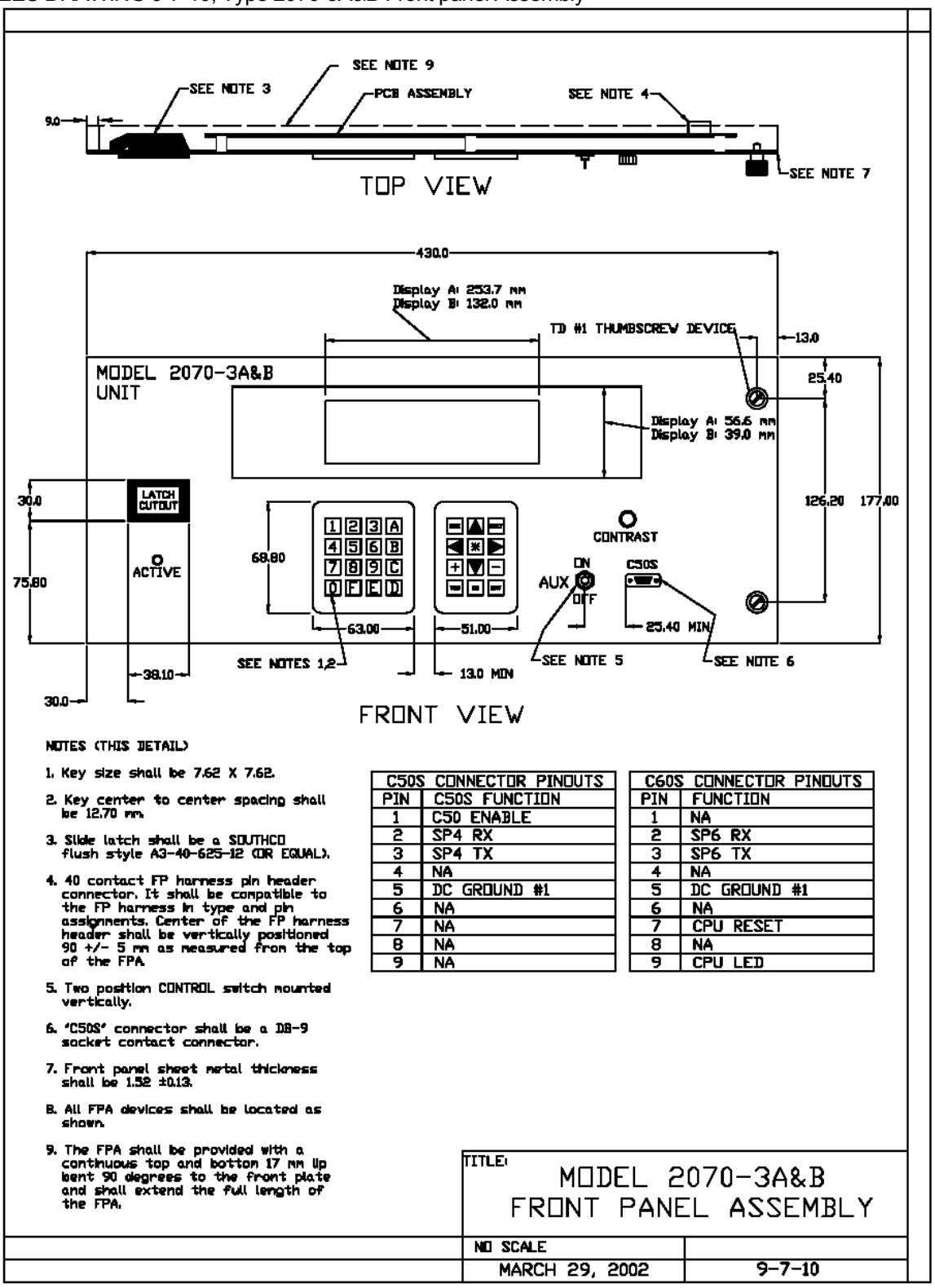
NO SCALE

MARCH 29, 2002

9-7-9

Figure 9-58: TEES DRAWING 9-7-9, Type 2070-2A Field I/O Module C1 & C11 Connectors

9.7.10 TEES DRAWING 9-7-10, Type 2070-3A&B Front panel Assembly



NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. Center of the FP harness header shall be vertically positioned 90 +/- 5 mm as measured from the top of the FPA.
5. Two position CONTROL switch mounted vertically.
6. 'C50S' connector shall be a DB-9 socket contact connector.
7. Front panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60S CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:
MODEL 2070-3A&B
FRONT PANEL ASSEMBLY

NO SCALE | MARCH 29, 2002 | 9-7-10

Figure 9-59: TEES DRAWING 9-7-10, Type 2070-3A&B Front panel Assembly

9.7.11 TEES DRAWING 9-7-11, Type 2070-3 Front Panel Assembly Key Codes

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	0D

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
NO SCALE	
MARCH 29, 2002	9-7-11

Figure 9-60: TEES DRAWING 9-7-11, Type 2070-3 Front Panel Assembly Key Codes

9.7.12 TEES DRAWING 9-7-12, Type 2070-3 Front Panel Assembly Key Codes

9.7.12.1 Page 9-7-12 changes: The display support of Reverse Video and Underline by the FPA is optional at vendor's choice.

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Move cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn…f	1B 50 P1 5B Pn 3B…Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 5B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A & B.
Commands shall be available for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;…P6 R	1B 5B P1 3B P2 3B…P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES

NO SCALE

MARCH 29, 2002 9-7-12

Figure 9-61: TEES DRAWING 9-7-12, Type 2070-3 Front Panel Assembly Key Codes

9.7.12.2 TEES DRAWING 9-7-13 Type 2070-4 Power Supply Module.

9.7.12.2.1 TEES 9-7-13 Notes addition: Termination identification labels for the connection pins of PS1 and PS2 harnesses shall be stenciled at both ends of the harnesses on the PS, MN, and VME buss

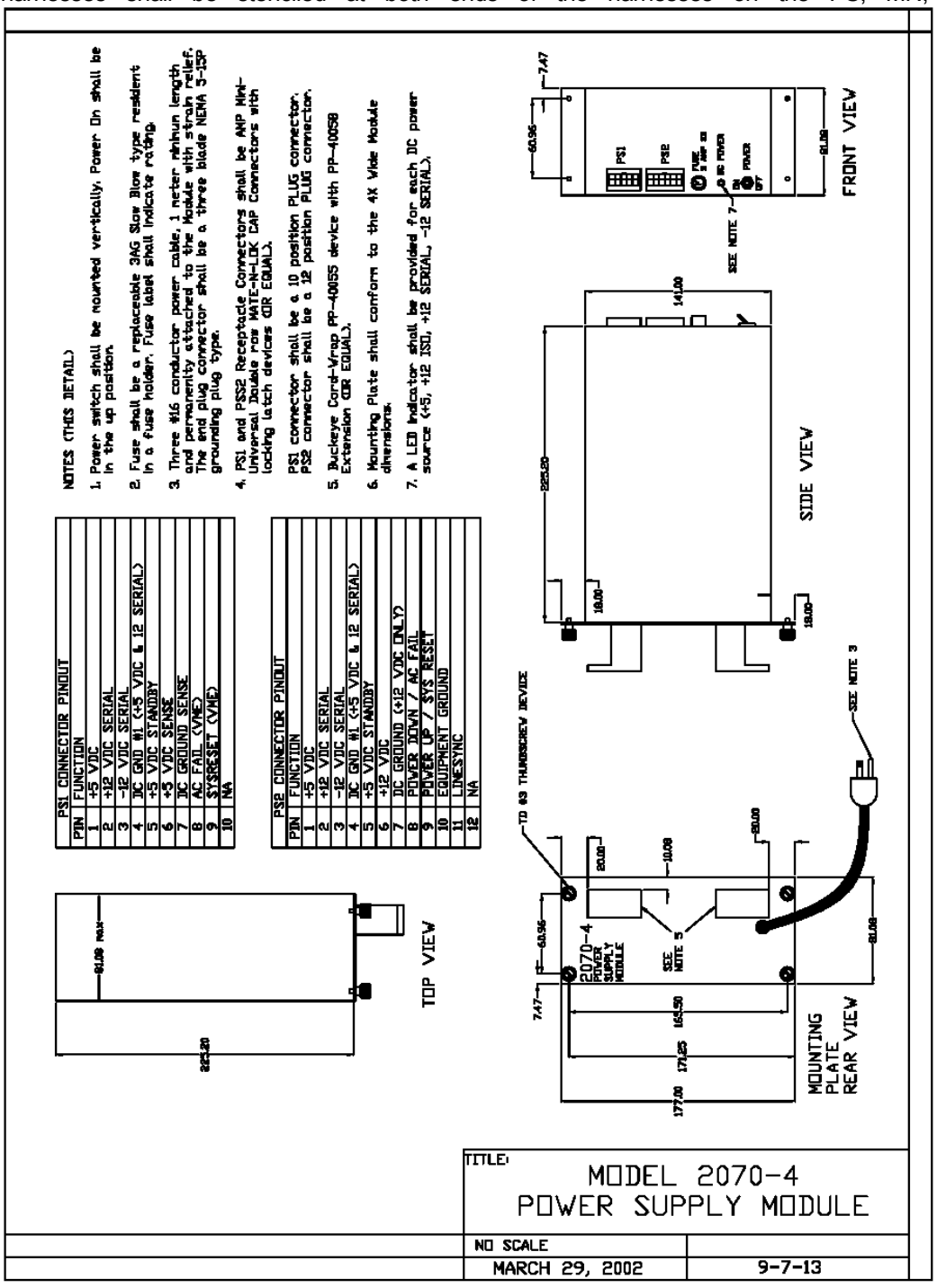


Figure 9-62: TEES DRAWING 9-7-13 Type 2070-4 Power Supply Module

9.7.13 TEES DRAWING 9-7-14, Type 2070-5 VME Cage Assembly

9.7.13.1 Note: All dimensions are in millimeters.

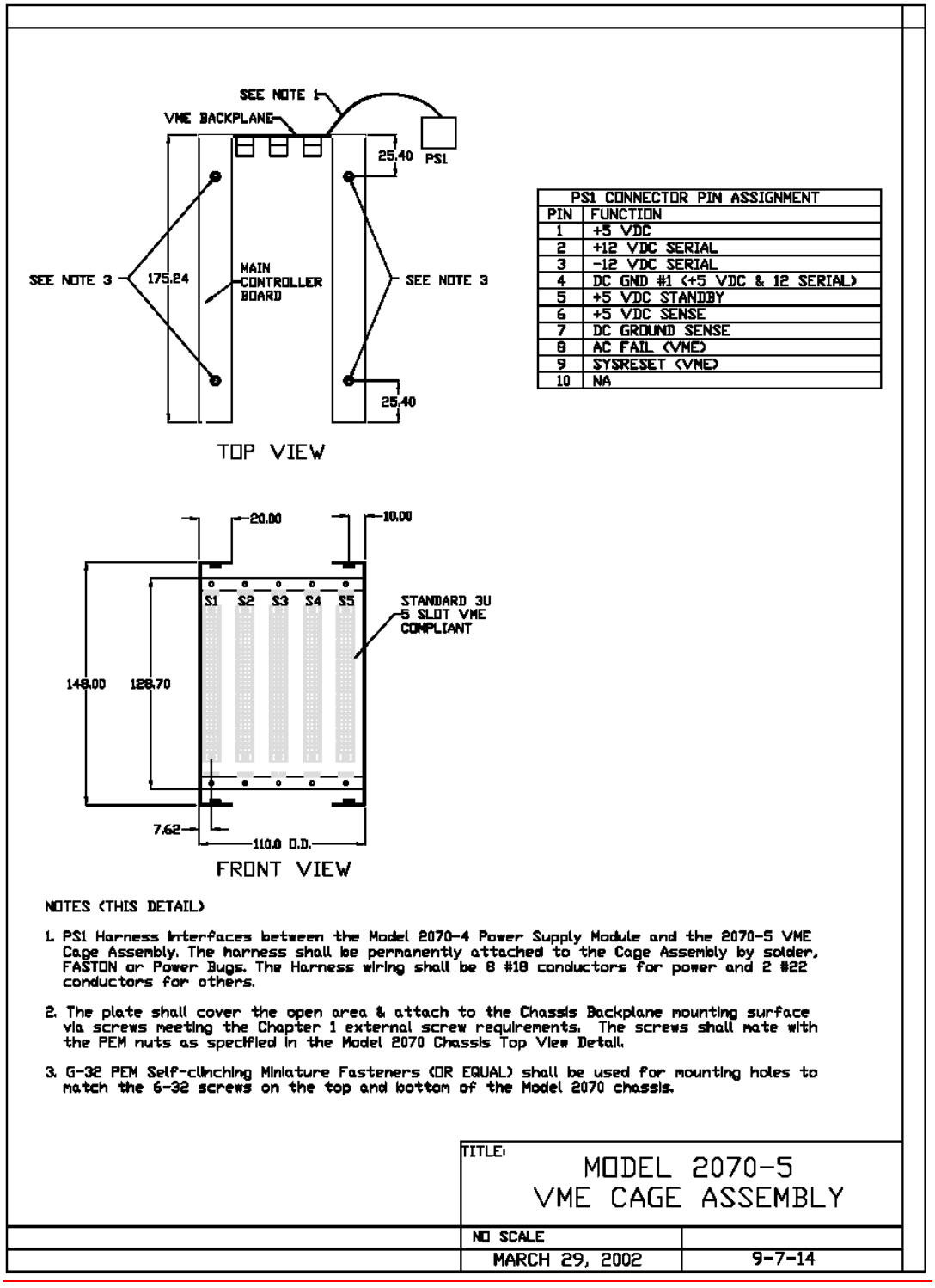


Figure 9-63: TEES DRAWING 9-7-14, Type 2070-5 VME Cage Assembly

CHAPTER 10 MODEL 2070 PERIPHERAL EQUIPMENT AND THE MODEL 2070N CONTROLLER UNIT

Note: Changes from the Caltrans Specification, Dated Nov. 19, 1999 are indicated as follows:

TEXT	MEANING
Red Text	Text Added.
Normal Text	Text from Caltrans Specification, Dated MARCH 29, 2002
~~Strikethrough Text~~	Deleted Text

Section 1 GENERAL NOTES:

10.1.1 The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). The Disable line shall be pulled up on the module.

10.1.2 Line drivers/receivers shall be socket mounted.

10.1.3 Isolation circuitry shall be opto- or capacitive-coupled isolation technologies.

10.1.4 Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.

10.1.5 The Comm modules shall be "Hot" swappable without damage to circuitry or operations.

10.1.6 The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). The Disable line shall be pulled up on the module.

Section 2 MODEL 2070-6 A & B ASYNC/MODEM SERIAL COMM MODULES

10.2.1 A fused isolated +5 VDC with a minimum of 100 mA power supply shall be provided for external use.

10.2.2 Three LOGIC switches per circuit shall be provided (faceplate mounted).

10.2.2.1 One shall be used to vertically switch between Half Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.2.2.2 A MODEM ENABLE switch shall be provided that when in UP Position shall enable the MODEM and in DOWN Position disable it.

10.2.2.3 A CONTROL switch shall be provided on the module front panel to turn ON (Up) / OFF (Down) all module power.

10.2.3 Two circuits designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector). The Circuits shall convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.

10.2.3.1 Each CIRCUIT shall have a MODEM with the following requirements:

1. Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.
2. Modulation: Phase coherent frequency shift keying (FSK).
3. Data Format: Asynchronous, serial by bit.
4. SPACE, ±1% tolerance. 2070-6B: 11.2 KHz MARK and 17.6 KHz SPACE, ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz& .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.
5. Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dBm (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.
6 Receiver Input Sensitivity: 0 to -40 dBm.
7. Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.
8. Clear-to-Send (CTS) Delay: 11 ±3 ms
9. Receive Line Signal Detect Time: 8 ±2 ms mark frequency.
10. Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).
11. Soft Carrier Turn Off Time: 10 ±2 ms (0.9 KHz for 2070-6A and 7.8 KHz for2070-6B). When the RTS is unasserted , the carrier shall turn off or go to soft carrier frequency.
12. Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.
13 Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.
14. Transmit Noise: Less than –50m dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.
15. Modem interface: EIA-232 Standards.

10.2.4 An on-board DIP-switch shall be provided on each modem to enable/disable the anti-streaming function. The anti-streaming function shall limit the modem's transmitter to be on for not more than 7 seconds. However, the 7-second timeout counter shall be reset and the transmitter shall be turned on when either the RTS line is asserted or new data (with RTS is still on) from the CPU are received.

Section 3 MODEL 2070-7A & 7B ASYNC SERIAL COMM MODULE

10.3.1 Two circuits designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).

10.3.2 2070 -7A Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

10.3.3 2070: 7B Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

10.3.4 Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled to function.

Section 4 MODEL 2070-2A FIELD I/O MODULE

10.4.1 The Model 2070-2A Module shall be a 2X wide PCBA Type.

10.4.2 The C12S Connector shall be mounted on the module front panel. The connector type shall be a DB-25 socket connector with pin assignments as follows:

PIN	FUNCTION	PIN	FUNCTION
1	TX DATA+	14	TX DATA-
2	DC GROUND #2	15	DC GROUND #2
3	TX CLOCK+	16	TX CLOCK-
4	DC GROUND #2	17	DC GROUND #2
5	RX DATA+	18	RX DATA-
6	DC GROUND #2	19	DC GROUND #2
7	RX CLOCK+	20	RX CLOCK-
8	LINESYNC+	21	LINESYNC-
9	POWER UP+	22	POWER UP-
10	POWER DOWN+	23	POWER DOWN-
11	NA	24	NA
12	NA	25	EQUIP GND
13	NA		

Figure 10-1: CONNECTOR C12S PIN ASSIGNMENTS

10.4.3 The module's functions are to isolate (Chapter 9 Section 3 Isolation Specification applies) the EIA-485 internal signal line voltages between the CPU Module and external equipment, and drive/receive interface between said devices. The line drivers/receivers shall be capable of interfacing and operating with external devices up to 1,000 meters away. The line drivers/receivers shall be CMOS devices and socket mounted.

Section 5 MODEL 2070N CONTROLLER UNIT

10.5.1 **GENERAL**

10.5.1.1 The Model 2070-8 NEMA Interface Module Chassis and 2070N Back Cover shall be made of 1.524 mm minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

10.5.1.2 A permanent label shall be affixed to the Model 2070-8 Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

10.5.2 **MODEL 2070-8 NEMA INTERFACE MODULE**

10.5.2.1 The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors.

10.5.2.2 The Module Front Panel shall be furnished with the following:

1. ON/OFF POWER Switch mounted vertically with ON in the UP position.
2. LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 5% and the +24 VDC is within 8%.
3. Incoming VAC fuse protection.
4. Two DB-25S COMM connectors labeled "EX1" & "EX2."
5. Four NEMA Connectors A, B, C, & D.

10.5.2.3 A MODULE POWER SUPPLY shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

10.5.2.3.1 Specification 9.5.3 above INPUT PROTECTION

10.5.2.3.2 Specification 9.5.6 POWER SUPPLY REQUIREMENTS except Spec 9.5.6.3.

10.5.2.3.3 DC Voltage tolerances shall be ±3 %.

10.5.2.4 The supplied incoming AC Power shall be derived from Connector A Pins "p" (AC) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN."

10.5.2.5 AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

10.5.2.6 A MODULE PC Boards shall be mounted vertically.

10.5.2.7 *Power Down, NRESET, and LINESYNC shall be routed to the module via C12 Connector. The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH shall be an open circuit.

10.5.2.8 The Model 2070-8 NEMA Interface Module shall meet all requirements under CHAPTER 9 SECTION 3 with the following exceptions:

10.5.2.8.1 PARALLEL PORTS: 118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12 and Ground False, "0," exceeds 16.0 VDC. LINESYNC signal is incoming in differential logic.

10.5.2.8.2 SERIAL COMMUNICATION CIRCUITRY: The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. All signal lines shall be isolated. HAR 1 Harness shall be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to the Controller interface, the EIA-485 Signal lines shall be routed to EX1 Connector. All necessary driver/receiver and isolation circuitry shall be provided.

10.5.2.8.3 An EIA-232 Serial Port shall be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector.

10.5.2.9 A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces with the 2070 UNIT and the outside world.

10.5.2.10 FAULT and VOLTAGE MONITOR circuitry – NEMA TS1 and TS2 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) shall be provided.

10.5.2.11 Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24VDC) state.

10.5.2.11.1 The FCU Port 10, Bit 7 output shall normally change its state every 100 ms. A MODULE Watchdog (WDT) circuit shall monitor the output. No state change for 2 □0.1 seconds shall cause the circuit output

to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

10.5.2.11.2 The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC ("0.25). If the voltage exceeds the limits, the circuit output shall generate a FALSE output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

10.5.2.11.3 The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

10.5.2.11.4 CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

10.5.2.11.5 CPU / FCU operation at POWER UP shall be as follows:

1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
2. CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responses to CPU with "E" bit set.
3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
4. * If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
5. This is operational and preceded User Software.

10.5.2.11.6 A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in FALSE state.

10.5.3 The 2070N Back Cover shall be provided to protect the interface harnesses. The Back Cover shall be delivered attached to the 2070 ATMS Controller Unit and 2070-8 NEMA Interface Module per Section 5.

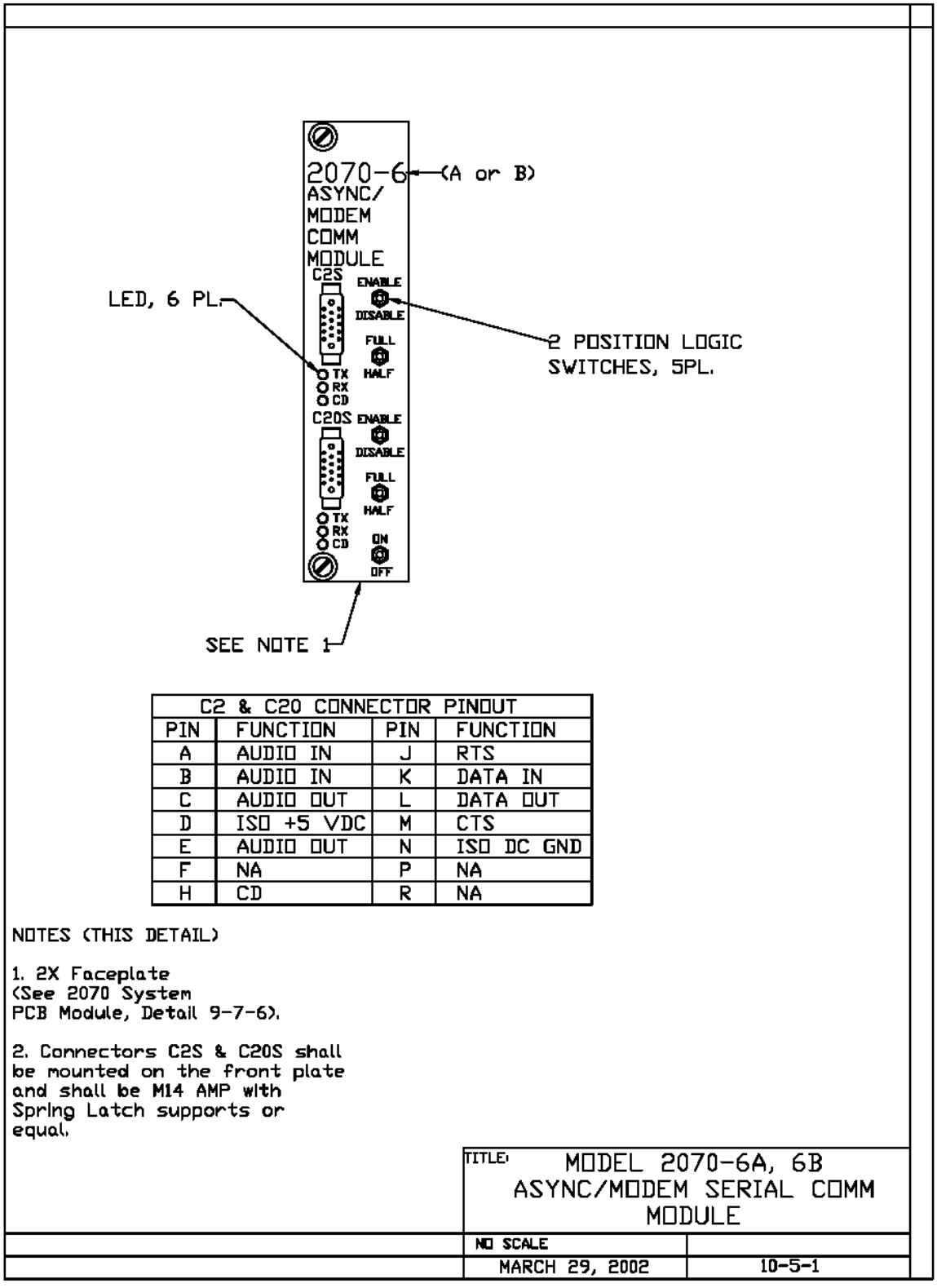
Section 6 CHAPTER DETAILS

10.6.1 Section Notes:

10.6.1.1 All dimensions are in millimeters.

10.6.1.2 Module sheet metal tolerance shall be 0.38 mm or less.

10.6.2 TEES DRAWING 10-5-1, MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE



C2 & C20 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	DATA IN
C	AUDIO OUT	L	DATA OUT
D	ISO +5 VDC	M	CTS
E	AUDIO OUT	N	ISO DC GND
F	NA	P	NA
H	CD	R	NA

NOTES (THIS DETAIL)

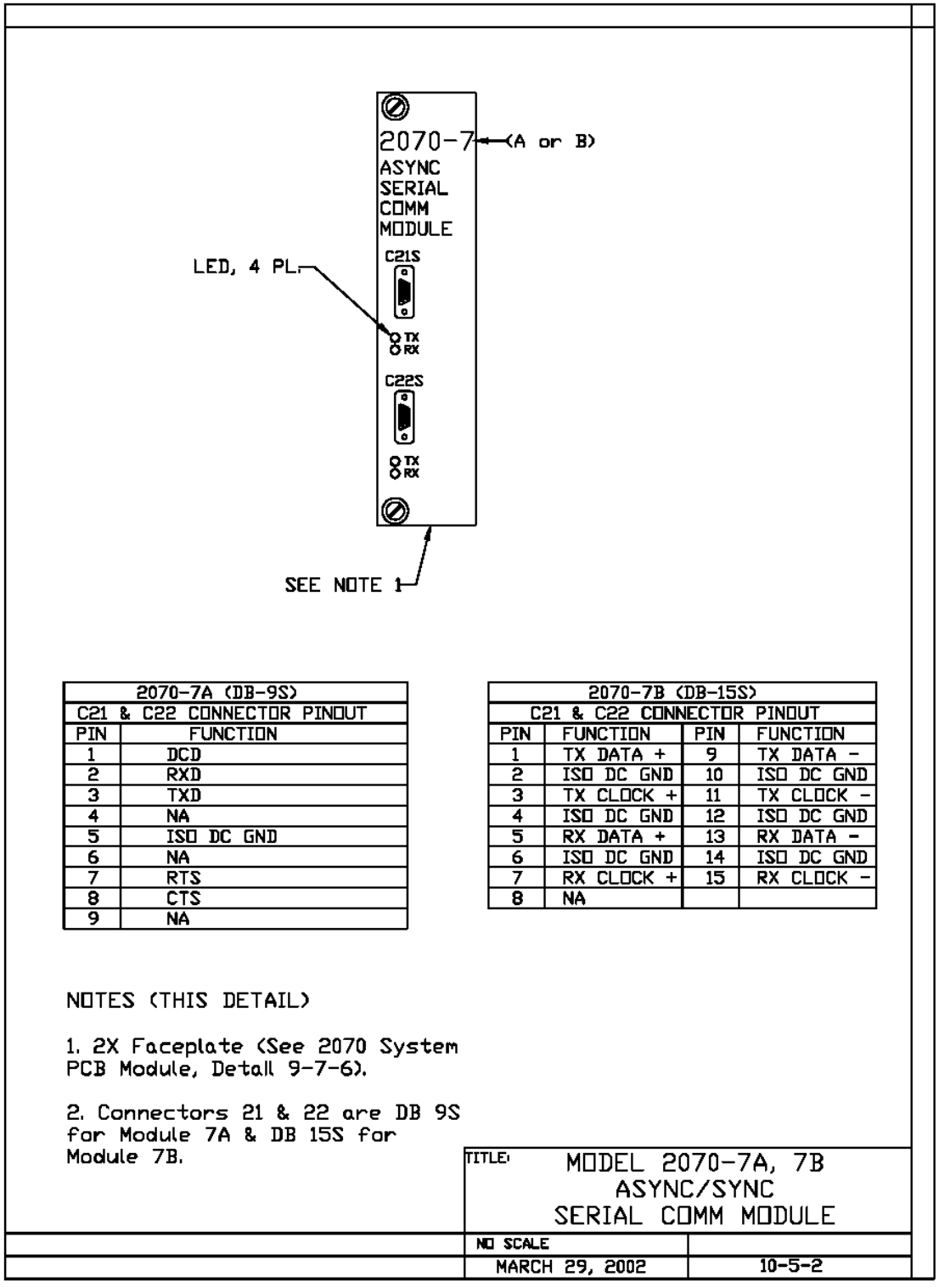
1. 2X Faceplate
(See 2070 System
PCB Module, Detail 9-7-6).

2. Connectors C2S & C20S shall
be mounted on the front plate
and shall be M14 AMP with
Spring Latch supports or
equal.

TITLE: MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE	
NO SCALE	
MARCH 29, 2002	10-5-1

Figure 10-2: MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE

10.6.3 TEES DRAWING 10-5-2, MODEL 2070-7A, 7B SERIAL COMM MODULE



2070-7A (DB-9S)	
C21 & C22 CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	ISO DC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DB-15S)			
C21 & C22 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA +	9	TX DATA -
2	ISO DC GND	10	ISO DC GND
3	TX CLOCK +	11	TX CLOCK -
4	ISO DC GND	12	ISO DC GND
5	RX DATA +	13	RX DATA -
6	ISO DC GND	14	ISO DC GND
7	RX CLOCK +	15	RX CLOCK -
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail 9-7-6).

2. Connectors 21 & 22 are DB 9S for Module 7A & DB 15S for Module 7B.

TITLE:	MODEL 2070-7A, 7B ASYNC/SYNC SERIAL COMM MODULE	
	NO SCALE	
	MARCH 29, 2002	10-5-2

Figure 10-3: MODEL 2070-7A, 7B SERIAL COMM MODULE

CHAPTER 11 2070 / NEMA STANDARD CONTROLLER UNITS

Note: Changes from the CALTRANS TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS March 29, 2002 Spec are indicated as follows:

TEXT	MEANING
Red Text	Added Text.
Normal Text	Text from Caltrans Specification, Dated March 29, 2002
~~Strikethrough Text~~	Deleted Text

Section 1 GENERAL

11.1.1 This specification covers two versions of 2070 / NEMA Standard Controller Units. The versions associate with NEMA TS1 and NEMA TS2 Type 1 Standards. They are as follows:

Model 2070 (V or L) N1 Controller Unit (TS1)
Model 2070 (V or L) N2 Controller Unit (TS2-1)

11.1.2 The MODEL 2070 (V or L) N1 CONTROLLER UNIT consists of:

Unit CHASSIS
2070- 1A or 1B CPU Module
2070-2B Field I/O Module
2070-3B Front Panel Module
2070-4N (A or B) Power Supply Module
(2070-5 VME Cage Assembly, if required)
2070-8 Field I/O Module

11.1.3 The MODEL 2070 (V or L) N2 CONTROLLER UNIT consists of:

Unit CHASSIS
2070-1A or 1B CPU Module
2070-2N Field I/O Module
2070-3B Front Panel Module
2070-4N (A or B) Power Supply Module
(2070-5 VME Cage Assembly, if required)

11.1.4 The Serial Port 5 Frame Address for 2070-2N and 2070-8 shall be “20”.

Section 2 2070-2N FIELD IO MODULE

11.2.1 The 2070-2N Field I/O Module provides a TS2-1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor Logic Output via 2070 Serial Port 5 and Output Frame Byte 9 Bit 6 to the NEMA TS2 Cabinet Monitor Unit (CMU).

11.2.2 The Module shall meet the 2070–2A Module Requirements with the following exceptions:

No C1, C11 and C12 Connectors on the front panel of the module
No 64 inputs / 64 outputs requirements
Serial Port 5 routed to the FCU MPU Device only
Serial Port 3 shall not have a disabling switch

11.2.3 The module shall be a 4X type board/front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a 15 Pin DB 15S C14 Connector.

11.2.4 Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle. Connector A shall be a NEMA TS2 Type 1 (MS3106O-18-1S).

11.2.5 The module shall isolate 2070 Serial Port 3 from the Ax Connector and reconvert the lines to external ETA 485 drivers/receivers, which shall be terminated at C14 Connector. The Port shall be clocked at 153.6 Kbps.

11.2.6 An FCU output shall drive a open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 ma at 30 VDC.

11.2.7 Connectors A and C14 pin out and functions are as follows:

CONNECTOR A					
Pin	Function	Pin	Function	Pin	Function
A	AC Neutral	E	NA	I	NA
B	NA	F	Fault Monitor	J	NA
C	AC Line	G	DC#2 Ground		
D	NA	H	Equip Ground		

Figure 11-1: CONNECTOR A PIN OUT

CONNECTOR C14S:					
Pin	Function	Pin	Function	Pin	Function
1	TX Data+	6	DC Ground	11	TX Clock -
2	DC Ground	7	RX Clock +	12	Equip Ground
3	TX Clock+	8	DC Ground	13	RX Data -
4	DC Ground	9	TX Data:	14	NA
5	RX Data+	10	NA	15	RX Clock –

Figure 11-2: CONNECTOR C14S PIN OUT

11.2.8 Serial Port 3 shall control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards.

11.2.9 **2070-4N (A or B) POWER SUPPLY MODULE**

11.2.9.1 The 2070-4N Power Supply Module supports the NEMA TS 1 and TS2 Standards. The module is identical to the 2070-4N (A and B) Power Supply Requirements except for the following:

11.2.9.2 The power cord shall have a 15 inch ± 1 inch length as measured from the panel to the plug tips.

11.2.9.3 The AC Power Fail voltage shall be 85VAC ±2VAC.

11.2.9.4 The AC Power Restore voltage shall be 90VAC ±2VAC.

11.2.9.5 The 2070-4N (A or B), power supply shall have proper marking Example “2070 4N (A or B)”. A permanent sticker shall be an acceptable marking method.

Section 3 MODEL 2070- 8 FIELD I/O MODULE

11.3.1 The Module shall CONSIST OF the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS shall be made of 1.524-mm minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

11.3.2 The MODULE FRONT PANEL shall be furnished with the following:

ON/OFF POWER Switch mounted vertically with ON in the UP position.
LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 5% and the +24 VDC is within 8%.
Incoming VAC fuse protection.
Two DB-25S COMM connectors labeled "EX1" & "EX2."
Four NEMA Connectors A, B, C, & D.

11.3.3 A permanent LABEL shall be affixed to the Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

11.3.4 A MODULE POWER SUPPLY shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

11.3.4.1 Specification 9.5.3 INPUT PROTECTION

11.3.4.2 Specification 9.5.6 POWER SUPPLY REQUIREMENTS except Spec 9.5.6.3.

11.3.4.3 DC Voltage tolerances shall be ±3 %.

11.3.5 The supplied INCOMING AC POWER shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

11.3.6 All MODULE PC Boards shall be mounted vertically.

11.3.7 Power Down, NRESET, and LINESYNC shall be routed to the module via C12 Connector. The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH shall be an open circuit.

11.3.8 The Module shall meet all requirements under CHAPTER 1Section 1 with the following exceptions:

11.3.8.1 PARALLEL PORTS: 118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12 and Ground False, "0," exceeds 16.0 VDC. LINESYNC signal is incoming in differential logic.

11.3.8.2 SERIAL COMMUNICATION CIRCUITRY: The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. All signal lines shall be isolated. HAR 1 Harness shall be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to the Controller interface, the EIA-485 Signal lines shall be routed to EX1 Connector. All necessary driver/receiver and isolation circuitry shall be provided.

11.3.9 An EIA-232 Serial Port shall be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector.

11.3.10 A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232Interfaces with the 2070 UNIT and the outside world.

11.3.11 FAULT and VOLTAGE MONITOR circuitry – NEMA TS1 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) shall be provided.

11.3.12 Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24VDC) state.

11.3.13 The FCU Port 10, Bit 7 output shall normally change its state every 100 ms. A MODULE Watchdog (WDT) circuit shall monitor the output. No state change for 2 _0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

11.3.14 The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (_0.25). If the voltage exceeds the limits, the circuit output shall generate a FALSE output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

11.3.15 The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

11.3.16 CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

11.3.17 CPU / FCU operation at POWER UP shall be as follows:

FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responses to CPU with "E" bit set.
Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
* If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
This is operational and preceded User Software.

11.3.18 A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in FALSE state.

Section 4 CHAPTER DETAILS

11.4.1 Section Notes:

11.4.1.1 All dimensions are in millimeters.

11.4.1.2 Module sheet metal tolerance shall be 0.38 mm or less.

11.4.2 TEES DRAWING 11-5-1, MODEL 2070N1 FRONT VIEW

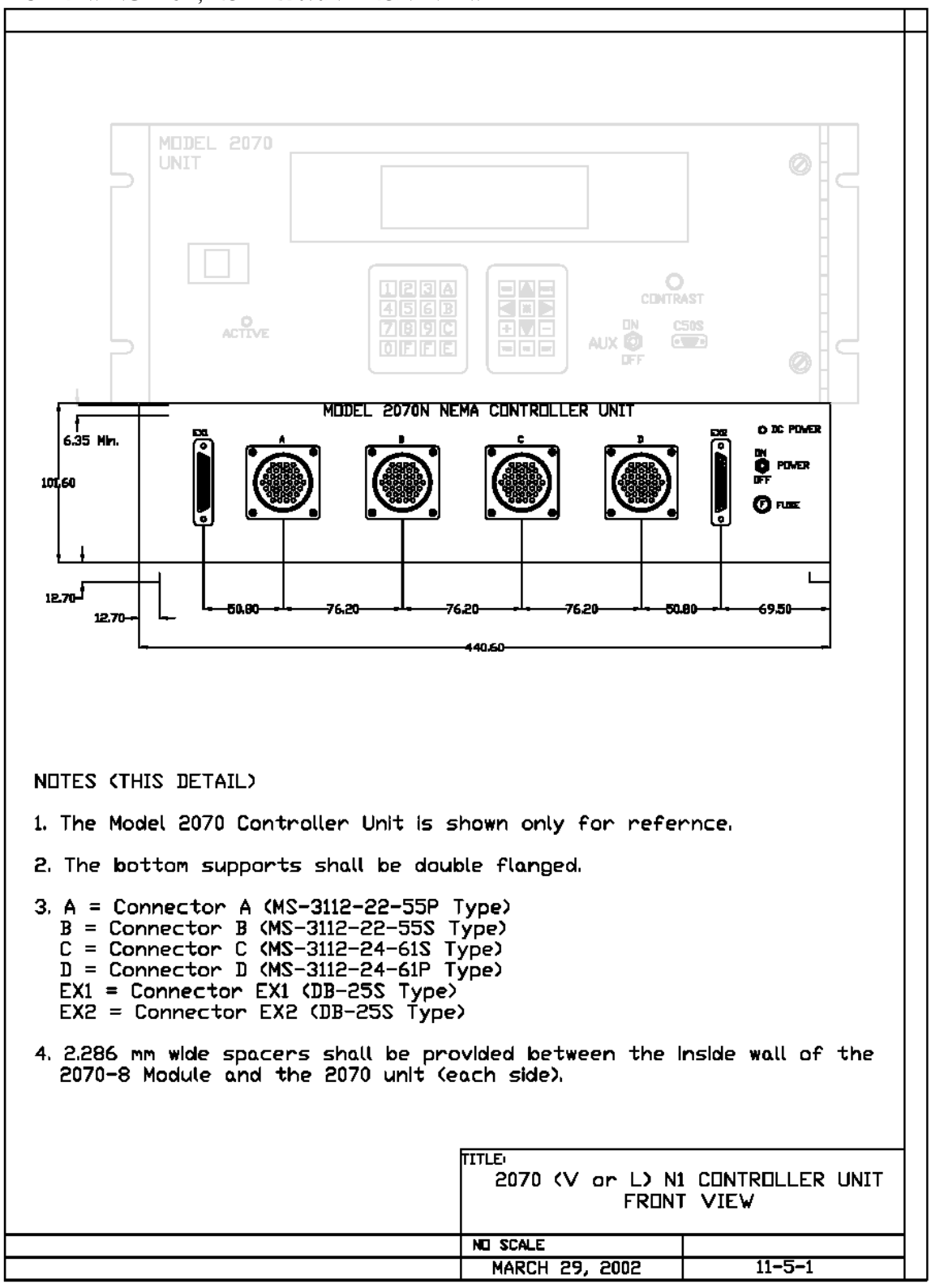


Figure 11-3: 2070 (V or L) N1 CONTROLLER UNIT, FRONT VIEW

11.4.3 TEES DRAWING 11-5-2,MODEL 2070N1 SIDE VIEW 11-5-2

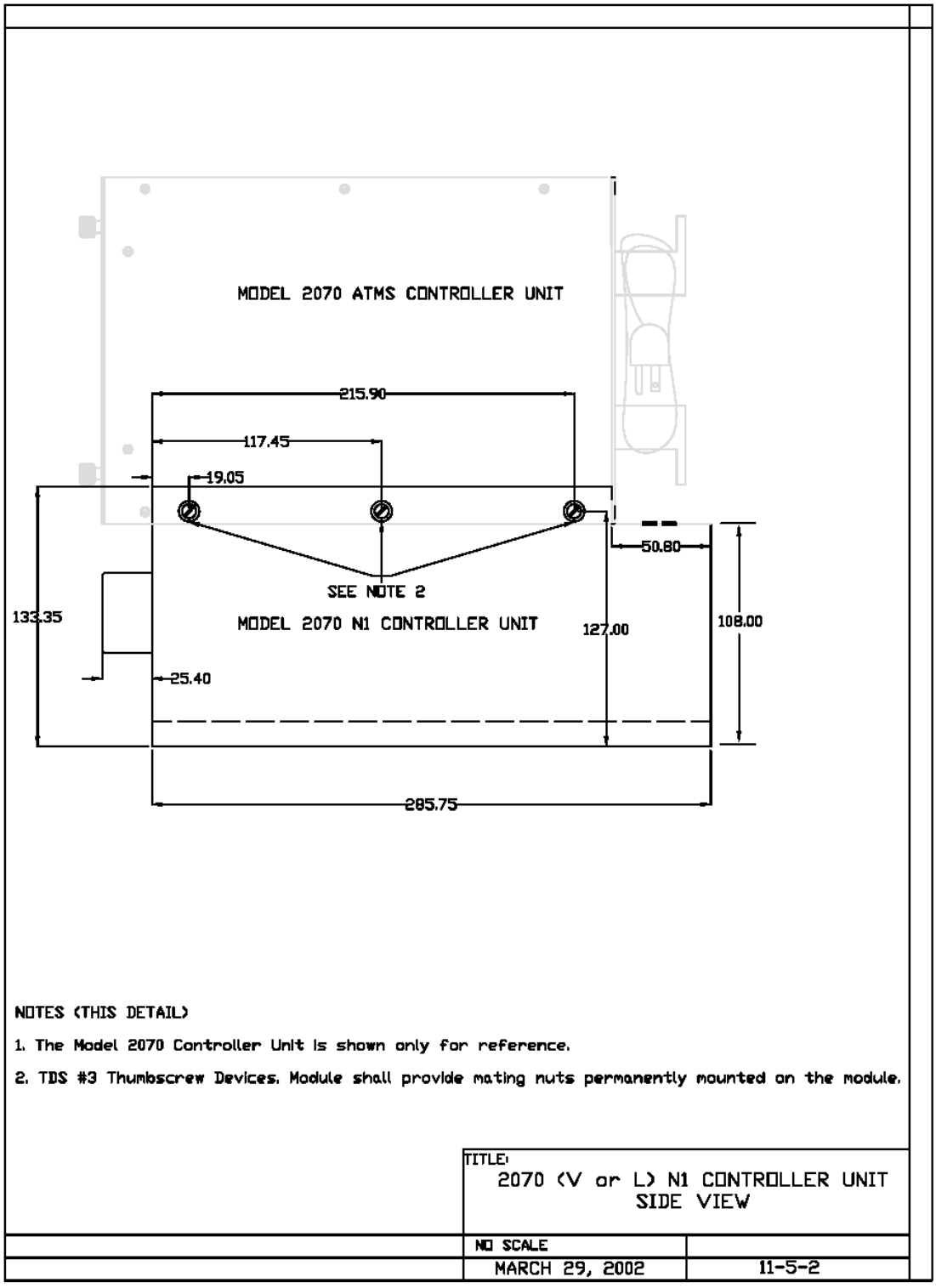


Figure 11-4: 2070 (V or L) N1 CONTROLLER UNIT, SIDE VIEW

11.4.4 TEES DRAWING 11-5-3, MODEL 2070N1 ISO VIEW 11-5-3

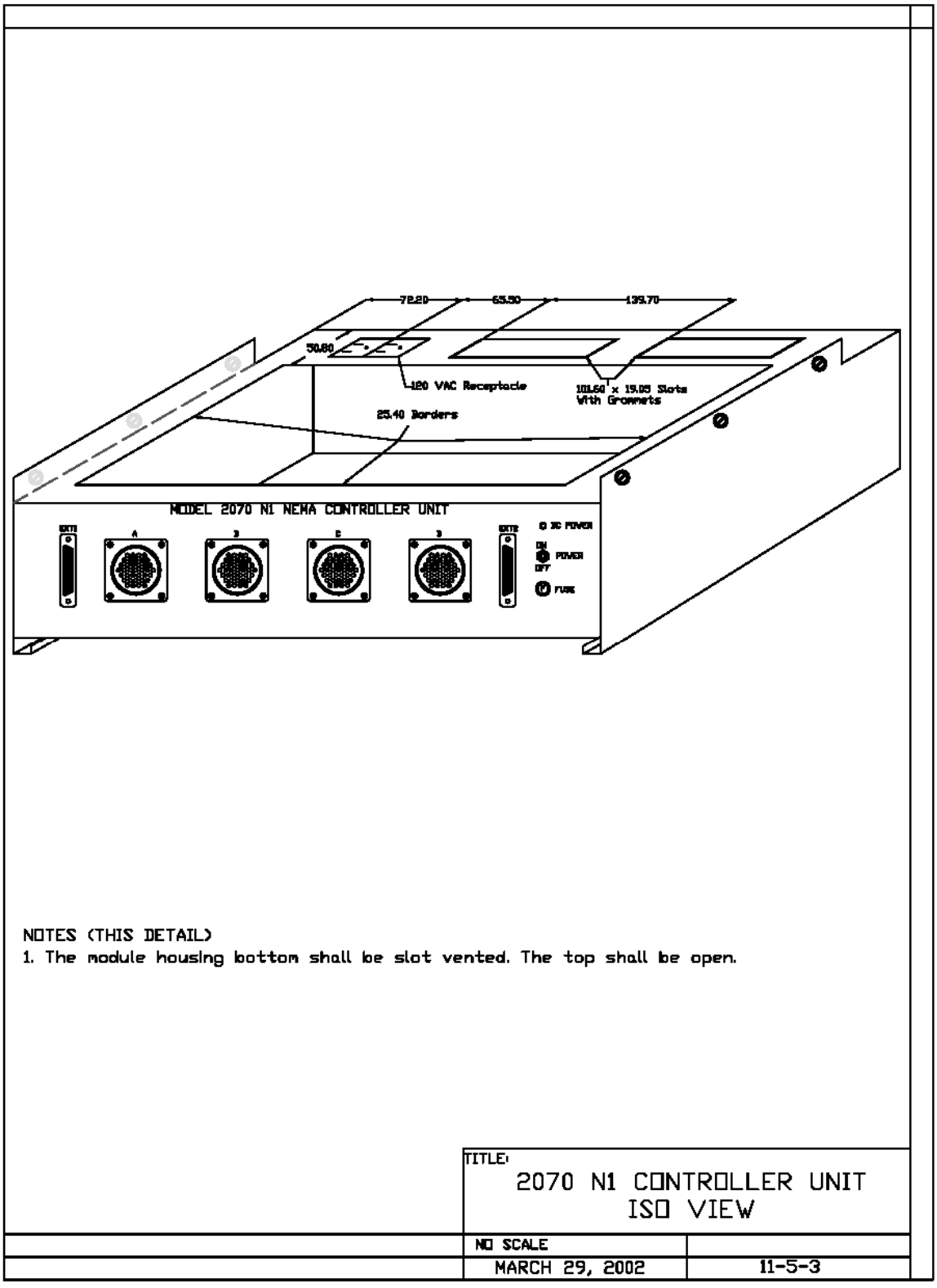


Figure 11-5: 2070 N1 CONTROLLER UNIT, ISO VIEW

11.4.5 TEES DRAWING 11-5-4, MODEL 2070N1 2070-8 FIELD I/O MODULE, CONN A & B 11-5-4

	CONNECTOR A			CONNECTOR B		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Fault Monitor	---	---	Phase 1 Next	Out	8-1
B	+24 VDC External	---	---	Reserved	In	9-5
C	Voltage Monitor	---	---	Phase 2 Next	Out	8-2
D	Phase 1 Red	Out	1-1	Phase 3 Green	Out	3-3
E	Phase 1 Don't Walk	Out	4-1	Phase 3 Yellow	Out	2-3
F	Phase 2 Red	Out	1-2	Phase 3 Red	Out	1-3
G	Phase 2 Don't Walk	Out	4-2	Phase 4 Red	Out	1-4
H	Phase 2 Ped Clear	Out	5-2	Phase 4 Ped Clear	Out	5-4
J	Phase 2 Walk	Out	6-2	Phase 4 Don't Walk	Out	4-4
K	Phase 2 Vehicle Detector	In	1-2	Phase 4 Check	Out	7-4
L	Phase 2 Pedestrian Detector	In	2-2	Phase 4 Vehicle Detector	In	1-4
M	Phase 2 Hold	In	3-2	Phase 4 Pedestrian Detector	In	2-4
N	Stop Timing (Ring 1)	In	6-2	Phase 3 Vehicle Detector	In	1-3
P	Inh Max Term (Ring 1)	In	6-3	Phase 3 Pedestrian Detector	In	2-3
R	External Start	In	8-1	Phase 3 Omit	In	5-3
S	Interval Advance	In	8-2	Phase 2 Omit	In	5-2
T	Indicator Lamp Control	In	8-3	Phase 5 Ped Omit	In	4-5
U	AC Neutral	---	---	Phase 1 Omit	In	5-1
V	Chassis Ground	---	---	Ped Recycle (Ring 2)	In	7-5
W	2070N DC Ground	---	---	Reserved	In	9-6
X	Flashing Logic Out	Out	11-7	Reserved	In	9-7
Y	Coded Status Bit C (Ring 1)	Out	12-3	Phase 3 Walk	Out	6-3
Z	Phase 1 Yellow	Out	2-1	Phase 3 Ped Clear	Out	5-3
a	Phase 1 Ped Clear	Out	5-1	Phase 3 Don't Walk	Out	4-3
b	Phase 2 Yellow	Out	2-2	Phase 4 Green	Out	3-4
c	Phase 2 Green	Out	3-2	Phase 4 Yellow	Out	2-4
d	Phase 2 Check	Out	7-2	Phase 4 Walk	Out	6-4
e	Phase 2 On	Out	9-2	Phase 4 On	Out	9-4
f	Phase 1 Vehicle Detector	In	1-1	Phase 4 Next	Out	8-4
g	Phase 1 Pedestrian Detector	In	2-1	Phase 4 Omit	In	5-4
h	Phase 1 Hold	In	3-1	Phase 4 Hold	In	3-4
i	Force Off (Ring 1)	In	6-1	Phase 3 Hold	In	3-3
j	Min Recall All Phases	In	8-4	Phase 3 Ped Omit	In	4-3
k	Manual Control Enable	In	8-5	Phase 6 Ped Omit	In	4-6
m	Call To Non-Actuated I	In	6-8	Phase 7 Ped Omit	In	4-7
n	Test Input A	In	9-1	Phase 8 Ped Omit	In	4-8
p	AC Power	---	---	Overlap A Yellow	Out	10-2
q	I/O Mode Bit A	In	8-6	Overlap A Red	Out	10-3
r	Coded Status Bit B (Ring 1)	Out	12-2	Phase 3 Check	Out	7-3
s	Phase 1 Green	Out	3-1	Phase 3 On	Out	9-3
t	Phase 1 Walk	Out	6-1	Phase 3 Next	Out	8-3
u	Phase 1 Check	Out	7-1	Overlap D Red	Out	11-6
v	Phase 2 Ped Omit	In	4-2	Reserved	In	9-8
w	Omit All-Red Clear (Phase 1)	In	6-7	Overlap D Green	Out	11-4
x	Red Rest Mode (Ring 1)	In	6-4	Phase 4 Ped Omit	In	4-4
y	I/O Mode Bit B	In	8-7	Not Assigned	---	---
z	Call To Non-Actuated II	In	7-8	Max II Selection (Ring 2)	In	7-6
AA	Test Input B	In	9-2	Overlap A Green	Out	10-1
BB	Walk Rest Modifier	In	9-4	Overlap B Yellow	Out	10-5
CC	Coded Status Bit A (Ring 1)	Out	12-1	Overlap B Red	Out	10-6
DD	Phase 1 On	Out	9-1	Overlap C Red	Out	11-3
EE	Phase 1 Ped Omit	In	4-1	Overlap D Yellow	Out	11-5
FF	Pedestrian Recycle (Ring 1)	In	6-5	Overlap C Green	Out	11-1
GG	Max II Selection (Ring 1)	In	6-6	Overlap B Green	Out	10-4
HH	I/O Mode Bit C	In	8-8	Overlap C Yellow	Out	11-2

TITLE:
2070-8 FIELD I/O MODULE
CONNECTORS A & B

NO SCALE

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Figure 11-6: MODEL 2070N1, 2070-8 FIELD I/O MODULE, CONN A & B

11.4.6 TEES DRAWING 11-5-5, MODEL 2070N1 2070-8 FIELD I/O MODULE, CONN C & D 11-5-5

	CONNECTOR C			CONNECTOR D		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Coded Status Bit A (Ring 2)	Out	12-4	Detector 9	In	10-1
B	Coded Status Bit B (Ring 2)	Out	12-5	Detector 10	In	10-2
C	Phase 8 Don't Walk	Out	4-8	Detector 11	In	10-3
D	Phase 8 Red	Out	1-8	Detector 12	In	10-4
E	Phase 7 Yellow	Out	2-7	Detector 13	In	10-5
F	Phase 7 Red	Out	1-7	Detector 14	In	10-6
G	Phase 6 Red	Out	1-6	Detector 15	In	10-7
H	Phase 5 Red	Out	1-5	Detector 16	In	10-8
J	Phase 5 Yellow	Out	2-5	Detector 17	In	11-1
K	Phase 5 Ped Clear	Out	5-5	Detector 18	In	11-2
L	Phase 5 Don't Walk	Out	4-5	Detector 19	In	11-3
M	Phase 5 Next	Out	8-5	Detector 20	In	11-4
N	Phase 5 On	Out	9-5	Detector 21	In	11-5
P	Phase 5 Vehicle Detector	In	1-5	Detector 22	In	11-6
R	Phase 5 Pedestrian Detector	In	2-5	Detector 23	In	11-7
S	Phase 6 Vehicle Detector	In	1-6	Detector 24	In	11-8
T	Phase 6 Pedestrian Detector	In	2-6	Clock Update	In	12-1
U	Phase 7 Pedestrian Detector	In	2-7	Hardware Control	In	12-2
V	Phase 7 Vehicle Detector	In	1-7	Cycle Advance	In	12-3
W	Phase 8 Pedestrian Detector	In	2-8	Max 3 Selection	In	12-4
X	Phase 8 Hold	In	3-8	Max 4 Selection	In	12-5
Y	Force Off (Ring 2)	In	7-1	Free	In	12-6
Z	Stop Timing (Ring 2)	In	7-2	Not Assigned	In	12-7
a	Inhibit Max Timing (Ring 2)	In	7-3	Not Assigned	In	12-8
b	Test Input C	In	9-3	Alarm 1	In	13-1
c	Coded Status Bit C (Ring 2)	Out	12-6	Alarm 2	In	13-2
d	Phase 8 Walk	Out	6-8	Alarm 3	In	13-3
e	Phase 8 Yellow	Out	2-8	Alarm 4	In	13-4
f	Phase 7 Green	Out	3-7	Alarm 5	In	13-5
g	Phase 6 Green	Out	3-6	Flash In	In	13-6
h	Phase 6 Yellow	Out	2-6	Conflict Monitor Status	In	13-7
I	Phase 5 Green	Out	3-5	Door Ajar	In	13-8
J	Phase 5 Walk	Out	6-5	Special Function 1	In	14-1
k	Phase 5 Check	Out	7-5	Special Function 2	In	14-2
m	Phase 5 Hold	In	3-5	Special Function 3	In	14-3
n	Phase 5 Omit	In	5-5	Special Function 4	In	14-4
p	Phase 6 Hold	In	3-6	Special Function 5	In	14-5
q	Phase 6 Omit	In	5-6	Special Function 6	In	14-6
r	Phase 7 Omit	In	5-7	Special Function 7	In	14-7
s	Phase 8 Omit	In	5-8	Special Function 8	In	14-8
t	Phase 8 Vehicle Detector	In	1-8	Preempt 1 In	In	15-1
u	Red Rest Mode (Ring 2)	In	7-4	Preempt 2 In	In	15-2
v	Omit All Red (Ring 2)	In	7-7	Preempt 3 In	In	15-3
w	Phase 8 Ped Clear	Out	5-8	Preempt 4 In	In	15-4
x	Phase 8 Green	Out	3-8	Preempt 5 In	In	15-5
y	Phase 7 Don't Walk	Out	4-7	Preempt 6 In	In	15-6
z	Phase 6 Don't Walk	Out	4-6	Alarm 1 Out	Out	12-7
AA	Phase 6 Ped Clear	Out	5-6	Alarm 2 Out	Out	12-8
BB	Phase 6 Check	Out	7-6	Special Function 1 Out	Out	13-1
CC	Phase 6 On	Out	9-6	Special Function 2 Out	Out	13-2
DD	Phase 6 Next	Out	8-6	Special Function 3 Out	Out	13-3
EE	Phase 7 Hold	In	3-7	Special Function 4 Out	Out	13-4
FF	Phase 8 Check	Out	7-8	Special Function 5 Out	Out	13-5
GG	Phase 8 On	Out	9-8	Special Function 6 Out	Out	13-6
HH	Phase 8 Next	Out	8-8	Special Function 7 Out	Out	13-7
JJ	Phase 7 Walk	Out	6-7	Special Function 8 Out	Out	13-8
KK	Phase 7 Ped Clear	Out	5-7	Not Assigned	---	---
LL	Phase 6 Walk	Out	6-6	Detector Reset	Out	11-8
MM	Phase 7 Check	Out	7-7	Not Assigned	---	---
NN	Phase 7 On	Out	9-7	+24 VDC	---	---
PP	Phase 7 Next	Out	8-7	2070N DC Gnd	---	---

TITLE: 2070-8 FIELD I/O MODULE CONNECTORS C & D

NO SCALE

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Figure 11-7: 2070-8 FIELD I/O MODULE CONNECTORS C & D

11.4.7 TEES DRAWING 11-5-6, MODEL 2070N1 2070-8 FIELD I/O MODULE, EX1 & EX2 CONNECTORS 11-5-6

EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD FCU
3	RXD FCU
4	RTS FCU
5	CTS FCU
6	NA
7	2070-8 DC GND
8	DCD FCU
9	2070-8 DC GND
10	485 TX Data+
11	485 TX Data-
12	485 TX Clock+
13	485 TX Clock-
14	2070-8 DC GND
15	485 RX Data+
16	485 RX Data-
17	2070-8 DC GND
18	485 RX Clock+
19	485 RX Clock-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD 1
3	RXD 1
4	RTS 1
5	CTS 1
6	NA
7	DC GND #1
8	DCD 1
9	AUDIO IN 1
10	AUDIO IN 1
11	AUDIO OUT 1
12	AUDIO OUT 1
13	NA
14	EQ GND
15	TXD 2
16	RXD 2
17	RTS 2
18	CTS 2
19	NA
20	DC GND #1
21	DCD 2
22	AUDIO IN 2
23	AUDIO IN 2
24	AUDIO OUT 2
25	AUDIO OUT 2

TITLE:
2070-8 FIELD I/O MODULE
EX1 & EX2 CONNECTOR

NO SCALE	
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Figure 11-8: 2070-8 FIELD I/O MODULE EX1 & EX2 CONNECTOR

CHAPTER 12 MODEL 2010 CONFLICT MONITOR UNIT

Section 1 SCOPE

12.1.1 This specification establishes minimum standards for Conflict Monitoring Devices designed for use with Model 2070, Model 170E-ATC and 170E Controllers, in Model 33x Traffic Signal Controller Cabinets supplied to the County of Los Angeles.

12.1.2 *NOTE: To use a Model 2010 with 170E or 170E-ATC Controllers, the controller's traffic signal program must sense and respond to FLASH SENSE (i.e. during FAULT RELAY RECOVERY flash). When FLASH SENSE ends, the controller must begin the Start Up Sequence, as if the controller had a long power down.*

12.1.3 The scope of this specification encourages development of new designs and enhancements. New designs may be submitted to the County for Acceptance Testing.

12.1.4 Reference is made to CHAPTER 1Section 1 (Scope). The County remains the sole judge on the ability of each device to meet specifications.

Section 2 GENERAL

12.2.1 The Model 2010 Monitor Unit is designed to be used with Model 2070 Controllers and Model 170, 170E, 170HC and 170E-ATC Controllers.

12.2.2 NOTE: To use a Model 2010 with 170 or 170E type controllers, the controller's traffic signal program must sense and respond to FLASH SENSE (i.e. during FAULT RELAY RECOVERY flash). When FLASH SENSE ends, the controller must begin the Start-Up Sequence, as if the controller had a long power down.

12.2.3 All monitored field output voltages shall be measured as true RMS (DC to 3 KHz), responsive to positive half-sine wave and negative half-sine wave as well as the full-sine wave.

12.2.4 Dimming algorithms (such as alternating or omitting a cycle) shall not compromise the monitor's ability to detect Fault conditions.

12.2.5 The Front Panel shall be removable without unsoldering connections.

12.2.6 **FAILED STATE OUTPUT CIRCUITS**:

12.2.6.1 An electro-mechanical relay shall be used to provide an output circuit during a Failed State. The relay contacts shall be normally closed (Failed State). In a NON-Failed State (relay coil energized), the contacts shall be open. The function of this output circuit is to energize the cabinet Mercury Contactor Coil and transfer field outputs from the Output File Load Switches to the Flasher Unit during a Failed State.

12.2.6.2 The relay contacts shall be rated for a minimum of 3 amperes at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 msec or less.

12.2.6.3 A second output circuit (Stop Time input to the controller unit) shall be provided separate from the Failed State Relay circuit. It shall be an optically coupled NPN Open Collector Transistor circuit rated for 30 VDC open collector and shall sink a minimum 50-mA load to less than 1.5 VDC in the active state. A blocking diode shall be provided on the transistor output to prevent it from sourcing power into the controller unit.

12.2.7 **MONITOR UNIT RESET**:

12.2.7.1 An Internal Reset (front panel momentary pushbutton switch labeled "RESET") and an External Test Reset input shall be provided to reset the Monitor to normal operation.

12.2.7.2 The Internal Reset switch shall be positioned so that it can be depressed while gripping the front panel handle.

12.2.7.3 The External Test Reset input line shall be optically isolated from the internal circuitry.

12.2.7.4 The monitor, once triggered by detection of a fault, shall remain in that state until a Reset Command is issued. Reset is issued only by the Internal Reset or by the External Test Reset input. A reset issuance by either source (Unit Reset) shall be trigged by only the leading edge (to prevent a constant reset from a switch failure or a constant external input).

12.2.8 **CONNECTORS**: Both Monitor Unit and Programming Card Connectors shall be PCB 28/56P Type. The connectors shall use the “bifurcated bellow” type contact or equivalent.

12.2.9 **DOOR AJAR CIRCUIT**: Pins 24 and 25 shall be connected together on the monitor PCBA at their connector fingers and be capable of carrying one ampere at +24 VDC.

12.2.10 **SOCKETS**: All device sockets used in the design of the monitor shall be of a type deemed highly reliable and approved by the County.

12.2.11 **HANDLE:** The top of the handle cannot be less then 4 inches below the top edge of the monitor front panel. Any other handle placement must have prior approval from The County.

12.2.12 **FUSE HOLDER:** Fuse holders on the front panel must be the low profile type. Fuses shall be 1 ¼” by ¼” in size.

12.2.13 **BATTERY:** A battery may not be used.

12.2.14 **EEPROM LABEL:** All UV erasable memory shall be protected from UV light. All microprocessors/microcontrollers and erasable memory with manufacturer’s firmware shale be labeled with their name and firmware revision.

12.2.15 **BLANK PCB:** One blank PCB shall be supplied for each revision and contract as a troubleshooting aid.

12.2.16 **INPUT IMPEDANCE** for all monitored AC inputs shall be 150K ohms (" 20%). These resistors shall be capable of dissipating ¼ watt each simultaneously.

Section 3 FUNCTIONAL

12.3.1 **GENERAL**

12.3.1.1 The monitor shall be fully operational over a voltage range of 85 VAC to 135 VAC.

12.3.1.2 The Conflict Monitor Unit is designed to monitor Green, Yellow, and Red AC circuits at the output terminals in Traffic Signal cabinets. In addition, the cabinet +24 VDC Supply, Special Function 1, Special Function 2. MC Coil (pin EE) and the Cabinet Controller Watchdog Signal outputs are also monitored. These signals are processed by the Monitor Unit circuitry, and if a failure is determined to have occurred, a relay output contact closure (FAILED STATE) places the cabinet and intersection in flashing operation.

12.3.1.3 The Conflict Monitor shall sense and respond to Conflicts and 24 VDC failures WHENEVER the AC line voltage is within the 85 VAC to 135 VAC operating range of the Monitor.

12.3.1.4 Means shall be provided to selectively inhibit monitoring of Yellow inputs (see YELLOW INHIBIT section 12.3.3.3 below).

12.3.1.5 Voltages appearing at the channel inputs shall be analyzed and acted upon regardless of their phase relationship to the AC line voltage.

12.3.1.6 Means shall be provided to review status of the Green, Yellow and Red inputs of all channels, at the time the fault was latched. Power loss shall not affect the retention of this data. Means shall be provided to selectively inhibit monitoring of Yellow inputs.

12.3.1.7 **ALL FAULTS SENSED BY THE MONITOR SHALL ONLY BE RESET BY THE FRONT PANEL RESET PUSHBUTTON OR EXTERNAL RESET INPUT!** In the event that the Monitor senses a fault, followed by a loss of operating voltage, the initial Failure Status shall be retained in memory and redisplayed after restoration of power.

12.3.1.8 It shall be possible to unplug the Monitor from the cabinet, and/or plug it in, without placing the cabinet into Flash operation, providing that the internal reset switch is held depressed while the unit is inserted. The Monitor shall begin normal operation in less than 1500 ms.

12.3.1.9 It shall be possible to unplug the Red Monitoring Connector, P20, or plug it in, without placing the cabinet into Flash operation.

12.3.1.10 If a microprocessor is used in the Monitor design, its program shall be written so that:

12.3.1.10.1 Integrity tests shall be performed on power up, on reset and periodically at least once every 2 seconds. The test includes testing every cell of memory, wrap-around test, and as much hardware as practical. A checksum of the (E) EPROM contents shall be stored in a section of the (E)EPROM, for comparison in the integrity tests.

12.3.1.10.2 Hardware external to the microprocessor circuits shall be employed to constantly sense proper microprocessor operation.

12.3.1.10.3 The monitor shall revert to Monitor Fail if a fault is detected with the microprocessor or during integrity tests.

12.3.1.10.4 The Monitor Fail condition shall not reset automatically when the fault condition goes away. A power off and on shall be required to clear the condition.

12.3.1.11 **MONITOR POWER:** The monitor shall not use current from the 24VDC input being sensed to power any of its internal circuitry. The watchdog signal, stop time, external reset, and 24VDC monitor input circuits shall be optically isolated from the monitor internal power supply.

12.3.1.12 **POWER FAIL**

12.3.1.12.1 A line voltage less than 85 VAC (± 2 V) for > 400 ms (± 100 ms) shall be considered a power failure. A power failure shall not result in resetting the monitor.

12.3.1.13 **POWER UP**(Note: see 12.3.1.8 above)

12.3.1.13.1 The Model 2010 Conflict Monitor shall be compatible with Model 170 controllers as well as the Model 2070 controller, which requires several seconds to power-up. When power is established (> 103 VAC ± 2V, for > 400ms ± 100ms), the 2010 will power up in the FAULT RELAY RECOVERY mode.

12.3.1.13.2 When power is established, FAULT RELAY RECOVERY shall be initiated. If the AC line voltage drops < 103 VAC (± 2V) for 400 ms (± 50ms), at any time during this period, the monitor returns to Fault Relay mode. For an interval of 4.0 seconds (± 0.5 seconds) the following will take place:

12.3.1.13.2.1 The Failed State Relay contacts remain closed.

12.3.1.13.2.2 All fault-monitoring functions remain suspended.

12.3.1.13.2.3 The AC POWER indicator light flashes at a 4 Hz (± 20%) rate with a 50 % duty cycle.

12.3.1.13.2.4 At the end of this time interval the Monitor begins counting watchdog signal transitions from the controller.

12.3.1.13.2.5 The resumption of normal fault monitoring shall follow Fault Relay Recovery When:

12.3.1.13.2.6 The monitor has counted 5 transitions between the True and False State from the watchdog signal OR 10 seconds (± has elapsed from the time that power is established.

12.3.1.13.2.7 If the watchdog signal does not become active, the monitor shall enter a WDT Error Failed State (Stop time output to the controller also becomes active).

12.3.2 **BASIC FEATURES (RED ENABLE OFF)**

12.3.2.1 The Conflict Monitor Unit operates as a State 210 CMU, The CMU monitors the cabinet for unsafe operation. If an unsafe condition exists, the Monitor will enter into a Failed State (see FAILED STATE OUTPUT CIRCUITS, Section 12.2.6 above). The BASIC FEATURES monitored shall be:

12.3.2.1.1 Conflict, 24 VDC fail, WDT error, conflict program card ajar, monitor failure and;

12.3.2.1.2 CONFIGURATION CHANGE FAULT – The monitor shall sense and respond to a change in the configuration of the monitor from the stored setting.

12.3.2.2 If for any reason a basic feature is disabled, the corresponding indicator will flash at 2 Hz ± 20% rate with 15% duty cycle.

12.3.3 **EXTENDED FEATURES** (see RED MONITORING section 12.3.8 below)

12.3.3.1 In addition to the features of the State Model 210 Monitor Unit, the 2010 Conflict Monitor Unit shall be designed to monitor Red circuits, multiple output failure, Lack-Of-Outputs failure and Yellow Interval Failure. These comprise the Extended Features. Special Function 1, Special Function 2 and MC Coil (pin EE) are also sensed.

12.3.3.2 To utilize Extended Features, the Monitor requires the RED ENABLE signal. Extended Features can be disabled by the MC Coil (pin EE) input. Extended Features apply only to channels selected for Red Monitoring by turning the channel's DIP-switch on.

12.3.3.3 YELLOW INHIBIT shall not disable Multiple Output and Lack-Of-Output Fail (Red Fail) monitoring on Green and Red on a channel(s) selected for extended features. When extended features are not utilized, the Red Fail indicator will flash at 2 Hz ±20% rate with a 15% duty cycle.

12.3.3.4 MULTIPLE OUTPUT FAIL: Simultaneous indication of Green, Yellow or Red field outputs on a single channel selected for extended features (see YELLOW FAIL 12.3.3.6 below).

12.3.3.5 LACK-OF-OUTPUT FAIL (RED FAIL): No active field outputs on a channel(s) selected for extended features.

12.3.3.6 YELLOW FAIL: The absence of a minimum period of active yellow field output during a green to red sequence.

12.3.4 **FRONT PANEL INDICATORS**

12.3.4.1 All indicator lights shall be water clear (not colored), not diffused lenses, Ultra-Bright, T-1 package LED's, Ledtech LT0373-41 (Red), LT0323-41 HE (Green) LT0333-41-UR (Yellow) or equivalent with a minimum luminous intensity of 100 mcd at 20 mA. Indicator lights shall be clearly visible in direct sunlight.

12.3.4.2 The AC POWER indicator shall be GREEN. Fault indicator lights shall be RED. Channel indicator lights shall be RED, unless there are three indicators per channel. In that case, each channel will have one red, one yellow, and one green indicator.

12.3.4.3 Indicator lights shall be arranged in a one vertical pattern with AC Power on top, Fault status lights as the upper indications, and the Channel lights as the lower indication's.

12.3.4.4 Where there are three indicators per channel, the indicators shall form three columns, with red to the left, yellow in the center and green to the right.

12.3.4.5 A Fault shall cause only the corresponding Fault indicator and appropriate channel indicators to display.

12.3.4.6 The indicators shall be labeled to provide the information described below:

12.3.4.6.1 **AC POWER**:

12.3.4.6.1.1 Shall illuminate when the AC Line Voltage exceeds 103 ± 2 VAC.

12.3.4.6.1.2 Shall FLASH at a 2 Hz ± 20% rate with a 50% duty cycle during **FALT RELAY MODE.**

12.3.4.6.1.3 Shall FLASH at a 4 Hz ± 20% rate with a 50% duty cycle during **FAULT RELAY RECOVERY.**

12.3.4.6.2 **VDC FAILED:** Shall illuminate when the Monitor has detected a 24 VDC failure.

12.3.4.6.3 **CONFLICT**: Shall illuminate when a conflicting signal condition has been detected. Active inputs shall be displayed on the channel indicators.

12.3.4.6.4 **WDT ERROR:** When the Watchdog Signal has ceased.

12.3.4.6.5 **CONFLICT PROGRAM CARD AJAR** (PC AJAR): Shall illuminate when the Conflict Program Card has been pulled out or is not properly seated in its slot. This indicator shall remain illuminated until the monitor is manually reset. The indicator shall flash at a 4 Hz ± 20% rate with 15% duty cycle to indicate CONFIGURATION CHANGE FAULT. The indicator shall flash in diagnostic mode to indicate previous faults (see 12.3.13 below)

12.3.4.6.6 **MONITOR FAILURE (MON FAIL):** A fault is detected within the operation of the monitor itself.

12.3.4.6.7 **LACK-OF-OUTPUT (RED FAIL):** Shall illuminate when the Monitor detects the absence of active output on any of the field outputs that comprise a monitored channel. The failed channel(s) shall be displayed on the corresponding channel indicator (s). When Red Monitoring is disabled, the indicator shall flash at 2 Hz ± 20% rate with 15% duty cycle.

12.3.4.6.8 **MULTIPLE OUTPUT (MULT IND):** Shall illuminate when the Monitor detects simultaneous on more than one of the field outputs that comprise a monitored channel (green, yellow, and red). The failed channel(s) shall be displayed on the corresponding channel indicators (s).

12.3.4.6.9 **YELLOW ERROR:** Shall illuminate when the monitor detects the absence of a minimum period of active yellow field output, during a green to red sequence. The failed channel shall be displayed on the corresponding channel indicator.

12.3.4.7 **CHANNEL INDICATORS**:

12.3.4.7.1 **ONE INDICATOR per CHANNEL:** Channel indicators shall illuminate to display presently active Green and Yellow inputs in normal operation. Following VDC Fail, Conflict, WDT Error and PC Ajar faults, indicators shall illuminate to display active inputs at the time of fault. Following Lack-Of-Output Fail, Multiple Output Fail or Yellow Error, indicators shall illuminate to display channel(s) with problem.

12.3.4.7.2 **THREE INDICATORS PER CHANNEL (optional):** Indicators shall illuminate to display all active channels in normal operation. Following VDC Fail, Conflict, WDT Error and PC Ajar faults, indicators shall illuminate to display active inputs at the time of fault. Following Lack-of-Output or Yellow faults, all 3 color indicators shall illuminate to display channel(s) with problem.

12.3.5 **CARD EDGE CONNECTOR PIN ASSIGNMENTS**

PIN	FUNCTION	PIN	FUNCTION
1	Channel 2 Green	A	Channel 2 Yellow
2	Channel 13 Green	B	Channel 6 Green
3	Channel 6 Yellow	C	Channel 15 Green
4	Channel 4 Green	D	Channel 4 Yellow
5	Channel 14 Green	E	Channel 8 Green
6	Channel 8 Yellow	F	Channel 16 Green
7	Channel 5 Green	H	Channel 5 Yellow
8	Channel 13 Yellow	J	Channel 1 Green
9	Channel 1 Yellow	K	Channel 15 Yellow
10	Channel 7 Green	L	Channel 7 Yellow
11	Channel 14 Yellow	M	Channel 3 Green
12	Channel 3 Yellow	N	Channel 16 Yellow
13	Channel 9 Green	P	(Not assigned)
14	(Not assigned)	R	Channel 10 Green
15	Channel 11 Yellow	S	Channel 11 Green
16	Channel 9 Yellow	T	(Not assigned)
17	(Not assigned)	U	Channel 10 Yellow
--		--	
18	Channel 12 Yellow	V	Channel 12 Green
19	(Not assigned)	W	(Not assigned)
20	Chassis Ground	X	(Not assigned)
21	AC-	Y	DC Ground
22	Watchdog Signal	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	Tied to Pin 25	BB	Stop Time (Output)
25	Tied to Pin 24	CC	(Not assigned)
26	(Not assigned)	DD	(Not assigned)
27	(Not assigned)	EE	Output Switch, Side #2
28	Output Switch, Side #1	FF	AC+
-- Slotted for keying between Pins 17 and 18 (Pins U and V)			

Figure 12-1: Model 2010 pin assignments.

12.3.6 **RED MONITORING CONNECTOR**

12.3.6.1 A connector (3M - 3428-5302, with two 3518 polarizing keys, or equivalent) shall be mounted on the Monitor front panel. Another connector of the same type, designated P20, is mounted near the rear of the cabinet output file. A ribbon cable 24 (±2) inches joins these connectors in length, provided with each unit. The connectors on the ends of the ribbon cable shall be of a closed type, to avoid electrical shock. The pin assignments of the P20 connector and terminal assembly shall be as shown below. Any P20 connector incorporating variations or additions to this specification shall be submitted to the County for approval prior to delivery of the sample unit.

12.3.7 P20 CONNECTOR PIN ASSIGNMENTS

PIN	FUNCTION	TERMINAL BLOCK	PIN	FUNCTION	TERMINAL BLOCK
1	Channel 15 Red	15	2	Channel 16 Red	16
3	Channel 14 Red	14	*4	Chassis Ground	17
5	Channel 13 Red	13	*6	Special Func.2	18
7	Channel 12 Red	12	*8	Special Func.1	19
9	Channel 10 Red	10	10	Channel 11 Red	11
11	Channel 9 Red	9	12	Channel 8 Red	8
13	Channel 7 Red	7	14	Channel 6 Red	6
15	Channel 5 Red	5	16	Channel 4 Red	4
17	Channel 3 Red	3	18	Channel 2 Red	2
19	Channel 1 Red	1	20	Red Enable	20

Figure 12-2: Model 2010 Red Monitoring Connector pin assignments.

12.3.7.1 Keying shall be between pins 3 & 5, and 17 & 19. (The odd numbered pins are on one side, and the even pins are on the other). The P20 connector and the CMU connector shall be keyed physically alike to prevent the Red Monitoring cable from being inserted into the P20 180 degrees out of alignment.

12.3.8 **RED ENABLE INPUT** (see RED ENABLE INPUT section 12.3.3 above)

12.3.8.1 Pin 20 of the Red Monitoring Connector shall provide the Red Enable input to the monitor. When the Red Monitoring Connector is disconnected, or Red Enable is not present, the Monitor shall function as a standard Model 210 Monitor, checking for conflicting Greens and/or Yellows, controller Watchdog signal, and cabinet +24VDC power supply. When enabled, all Monitor functions shall become active, including the Lack-of-Output, Multiple Output, and Yellow Fail capabilities of the monitor.

12.3.9 **SPECIAL FUNCTION 1 AND 2 INPUTS**

12.3.9.1 **SPECIAL FUNCTION 1** (Red Connector pin 8) An AC input to the monitor, which will DISABLE only the LACK-OF-OUTPUT (RED FAIL) monitoring functions wile it is active (e.g. during Railroad Preempt).

12.3.9.2 **SPECIAL FUNCTION 2** (Red Connector pin 6) Reserved for future use and shall be non-functional.

12.3.9.3 Means shall be provided to either select a PRESENCE of, or LACK of AC+ to enable these inputs.

12.3.10 **MONITORING OF CONFLICTING VOLTAGES**

12.3.10.1 Inputs to any channel, which are of sufficient level to exceed the set conflict threshold, shall be sensed as "ON" and shall illuminate their respective indicators.

12.3.10.2 The number of active channels shall in no way affect the conflict threshold or the level at which channels are sensed as "ON".

12.3.10.3 The following levels and times apply to full-wave, positive half-wave or negative half-wave inputs. The phase relationship of the input signals and the line voltage SHALL NOT affect the ability of the monitor to sense the defined input levels. For clarification of HALF-WAVE measurements, 15 Volts RMS is equivalent to a 21-Volt peak signal, and 25 Volts RMS is equivalent to a 35-Volt peak signal (sine wave input only).

12.3.10.4 Sensing of conflicting voltages, at the field terminals, of 25 Volts RMS or greater for a duration of 450 msec or longer shall cause a Failed State.

12.3.10.5 Sensing of conflicting voltages, at the field terminals, of 15 Volts RMS or less OR any voltage having duration of 200 msec or less shall NOT cause a Failed State.

12.3.10.6 Sensing of conflicting voltages, at the field terminals, of between 15 and 25 Volts RMS, OR any voltages sensed for duration between 200 and 450 msec MAY or MAY NOT cause a Failed State.

12.3.10.7 The watchdog, stop time, external reset, and 24V monitor input circuits shall be isolated from the conflict monitor internal power supply. Where the cabinet 24VDC-power supply is used to power these

circuits, it shall be conditioned to provide proper sense circuit operation, even under low voltage or high ripple conditions.

12.3.11 **CONFLICT PROGRAMMING CARD**

12.3.11.1 A plug-in PCBA Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically arranged and labeled for easy identification of the diodes by channel. With diodes in place, all output channels being monitored shall be in conflict. When the diode has been removed, the channels shall be interpreted as non-conflicting.

12.3.11.2 The programming card shall be 6 inches in depth and 5.15 to 5.30 inches in height, and shall intermate with a 28/56 pin double-sided connector having bifurcated contacts on 0.156-inch centers. The printed circuit board shall bisect its edge board fingers at their centers to within ±0.016 inches. The center of the edge board fingers shall be 2.6375 inches from either edge of the board. The programming card, when installed, shall be provided with card ejectors for removal from the front panel. It shall be flush with the front panel and slide smoothly on its track while being inserted into or removed from the monitor module.

12.3.11.3 PROGRAMMING CARD CONNECTOR PIN ASSIGNMENTS

Pin	FUNCTION (circuit side)	Pin	FUNCTION (component side)
1	Channel 2 Green	A	Channel 1 Green
2	Channel 3 Green	B	Channel 2 Green
3	Channel 4 Green	C	Channel 3 Green
4	Channel 5 Green	D	Channel 4 Green
5	Channel 6 Green	E	Channel 5 Green
6	Channel 7 Green	F	Channel 6 Green
7	Channel 8 Green	H	Channel 7 Green
8	Channel 9 Green	J	Channel 8 Green
9	Channel 10 Green	K	Channel 9 Green
10	Channel 11 Green	L	Channel 10 Green
11	Channel 12 Green	M	Channel 11 Green
12	Channel 13 Green	N	Channel 12 Green
13	Channel 14 Green	P	Channel 13 Green
14	Channel 15 Green	R	Channel 14 Green
15	Channel 16 Green	S	Channel 15 Green
16	DC GROUND	T	CONFLICT
17	Channel 1 Yellow	U	Channel 9 Yellow
18	Channel 2 Yellow	V	Channel 10 Yellow
19	Channel 3 Yellow	W	Channel 11 Yellow
20	Channel 4 Yellow	X	Channel 12 Yellow
21	Channel 5 Yellow	Y	Channel 13 Yellow
22	Channel 6 Yellow	Z	Channel 14 Yellow
23	Channel 7 Yellow	AA	Channel 15 Yellow
24	Channel 8 Yellow	BB	Channel 16 Yellow
--		--	
25	Not assigned	CC	Not assigned
26	Not assigned	DD	Not assigned
27	Not assigned	EE	Not assigned
28	Yellow Inhibit Common	FF	Not assigned
--			

Figure 12-3: Model 2010 Programming Card Connector pin assignments.

12.3.11.4 Pads for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin and the yellow inhibit common shall disable sensing the said channel yellow.

12.3.11.5 The programming card shall inter mate with a PCB 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provide a mechanically sound card and connector support including continuous card guides. When the programming card is resident in the unit, the card's front end shall be flush with the unit's front panel.

12.3.11.6 Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting Failed State.

12.3.12 **FAULT RELAY MODE**

12.3.12.1 **LINE DROP OUT:** The monitor will determine that a LINE DROP OUT has occurred when the AC Line Voltage is less then 98 ±2 VAC for more then 400 ± 50 ms.

12.3.12.1.1 Within this time frame the Monitor shall suspend all fault monitoring functions, close the Failed State Relay contacts and the AC POWER indicator will flash at a 2 Hz ± 20% rate, with a 50% duty cycle (to indicate the LINE DROP OUT status).

12.3.12.1.2 The monitor remains in the FAULT RELAY mode until a LINE RECOVERY has occurred.

12.3.12.2 **LINE RECOVERY**- The monitor will determine that a LINE RECOVERY has occurred when the AC line voltage is greater then 103 ± 2 VAC for more then 400 ± 50 ms (see FAULT RELAY RECOVERY 12.3.12.3 below).

12.3.12.3 **FAULT RELAY RECOVERY** – When LINE RECOVERY is established FAULT RELAY RECOVERY shall be initiated. If the AC line voltage drops less then 103 ± 2 VAC for more than 400 ± 50 ms during this period, the monitor returns to Fault Relay mode.

12.3.12.3.1 For an interval of 4.0 ± 0.5 seconds, the following will take place:

12.3.12.3.1.1 The Failed State Relay contacts remain closed. All fault-monitoring functions remain suspended. The AC POWER indicator light flashes at a rate of 4 Hz ± 20% rate with 50% duty cycle.

12.3.12.3.1.2 At the end of this time interval the Monitor begins counting watchdog signal transitions.

12.3.12.4 **RESUMPTION OF NORMAL MONITORING** – The resumption of Normal Monitoring shall follow Fault Relay Recovery when:

12.3.12.4.1 The monitor has counted 5 transitions between the True and False state of the watchdog signal **OR** 10 ± 0.5 seconds has elapsed from the time of LINE RECOVERY.

12.3.12.4.2 If the watchdog signal does not become active, the monitor shall into a WDT Error Failed State and the Stop Time output to the controller shall become active.

12.3.12.5 **RED MONITORING**: Monitoring the red inputs permit use of the EXTENDED FEATURES (see EXTENDED FEATURES section 12.3.3 above). Enabling the EXTENDED FEATURES are controlled by:

12.3.12.6 **RED ENABLE INPUT**: When ON, enables EXTENDED FEATURES for all channels selected for RED MONITORING. When OFF, the monitor performs only Basic Features (see RED ENABLE INPUT 12.3.8 above).

12.3.12.7 **CHANNEL DIP SWITCHS:** Selects EXTENDED FEATURES on a per channel basis, when RED ENABLE INPUT is also on.

12.3.12.8 **MC COIL INPUT (PIN EE):** The monitor shall disable Extended Features when activation of the MC Coil is detected, not initiated by the monitor (typically caused by the cabinet being in maintenance flash.

12.3.12.9 **SPECIAL FUNCTION 1 and 2 INPUTS** (see SPECIAL FUNCTION 1 and 2 INPUTS section 12.3.9 above).

12.3.13 **DIAGNOSTIC MODE**

12.3.13.1 The monitor shall provide a means of reviewing the current and two previous faults, as well as the active channels at those times. Review of three faults shall be possible. Power loss shall not affect the retention of this data.

12.3.13.2 The PC Ajar indicator shall flash to indicate which fault information is being displayed.

12.3.13.3 While displaying information from the current fault, PC Ajar indicator shall flash at 1 Hz ± 20% rate with 15% duty cycle.

12.3.13.4 While displaying information from the previous fault, the indicator shall pulse twice every second, 150 ms on, 150 ms off, 150 ms on, 550 ms off.

12.3.13.5 While displaying information from the fault before that, the PC Ajar indicator shall pulse three times per second, 150 ms on, 150 ms off, 150 ms on, 150 ms off, 150 ms on, 250 ms off.

12.3.14 **MONITOR CONFIGURATION**

12.3.14.1 All settings, permissives, yellow inhibits, DIP-switch settings for extended features, other dip switch settings, jumper settings (if any) must be clearly discernable visually on the monitor.

12.3.14.2 The monitor configuration shall be transferred to nonvolatile memory by pressing the reset switch for 5 seconds.

12.3.14.3 The monitor configuration will be compared to the stored configuration at power up, reset, and periodically, at least once every 2 seconds. A change in configuration shall cause a Configuration Change Fault.

12.3.14.4 Configuration of the monitor may not be done through external means.

Section 4 ELECTRICAL

12.4.1 **OPERATING RANGE**

12.4.1.1 The monitor shall be fully operational over a voltage range of 85 VAC to 135 VAC.

12.4.1.2 Below 85 ± 2 VAC > 400 ± 100 ms the monitor shall suspend fault monitoring, de-energize the FAILED STATE RELAY and extinguish the AC POWER indicator light.

12.4.2 **ISOLATION**: Chassis Ground and AC- shall be isolated from one another.

12.4.3 **MONITORED AC INPUTS**: The following voltage and time thresholds apply to all AC inputs, full wave, positive half-wave, negative half-wave inputs, alternating full-wave or other dimming algorithms.

12.4.3.1 Input Impedance for all monitored AC inputs shall be 150K ohms (" 20%). These resistors shall be capable of dissipating ¼ watt each simultaneously.

12.4.3.2 **GREEN AND YELLOW INPUTS**

Any inputs < 15 VRMS shall be considered OFF.
Any inputs > 25 VRMS shall be considered ON.

12.4.3.3 **RED, RED ENABLE AND SPECIAL FUNCTION INPUTS**

Any inputs < 50 VRMS shall be considered OFF.
Any inputs > 70 VRMS shall be considered ON.

12.4.3.4 **MC COIL INPUT (pin EE)**

Input < 50.0 VRMS shall be considered OFF.
Input > 70.0 VRMS shall be considered ON.

12.4.3.5 **TIMING OF CONFLICTING INPUTS OR MULTPLE INPUTS**

Inputs on < 200 msec shall be considered NO FAULT.
Inputs on > 450 msec shall be considered a FAULT.

12.4.3.6 **TIMING OF LACK-OF-OUTPUT (RED FAIL)**

Lack of output < 1200 ms shall be considered NO FAULT.
Lack of output > 1500 ms shall be considered a FAULT.

12.4.3.7 **TIMING OF YELLOW FAIL**

Duration of Yellow > (MIN YELLOW SETTING) shall be considered NO FAULT.
Duration of Yellow < (MIN YELLOW SETTING) shall be considered a FAULT

12.4.3.8 **MIN YELLOW SETTING** shall be adjustable from 2.7 seconds to at least 4 seconds, in 0.2 second increments. DIP switches shall be used to configure the MINMUM YELLOW SETTING.

12.4.3.8.1 The duration shall be actual yellow time, not measured from end of green to start of red.

12.4.4 **MONITORED DC INPUTS -**

12.4.4.1 **+24 VDC INPUT**

Input < 18VDC shall be considered a FAULT
Input > 22VDC shall be considered NO FAULT

12.4.4.2 **+24 VDC TIMING**

Input < 18 VDC for < 200 msec shall be considered NO FAULT. Input < 18 VDC for > 500 msec shall be considered a FAULT.

12.4.4.3 **WATCHDOG SIGNAL INPUT**

Input < 4 VDC shall be considered a LOW
Input > 12 VDC (or OPEN) shall be considered a HIGH

12.4.4.4 **WATCHDOG ERROR TIMING**

Lack of valid input signal changes for < 900 msec shall be considered NO FAULT
Lack of valid input signal changes for > 1100 msec shall be considered A FAULT

CHAPTER 13 TRAFFIC SIGNAL BATTERY BACK-UP SYSTEMS

Section 1 SCOPE

13.1.1 This specification establishes minimum standards for Battery Back-up Systems designed for use with Traffic Signal Controller Cabinets supplied to the County of Los Angeles.

13.1.2 The County remains the sole judge on the ability of each device to meet specifications.

Section 2 GENERAL

13.2.1 The Battery Back-up System (BBS) shall provide reliable emergency power to a traffic signal in the event of a power failure or interruption. That is, the BBS shall be capable of providing power for full run-time operation (Automatic Mode) for an "LED-only" intersection (all colors, red, yellow, and green, INCLUDING PEDESTRIAN INDICATIONS) or flashing mode (Red Flash Mode) operation for an intersection using Red LED's.

13.2.2 The BBS shall include, but not be limited to the following: inverter/charger, power transfer relay, batteries, a separate manually operated non-electronic bypass switch (see Figure 1 - BBS Block Diagram) and all necessary hardware and CONNECTING wiring.

Section 3 OPERATION

13.3.1 The BBS shall provide a minimum of two (2) hours of full run-time operation for a 700 Watt / 1000VA load (an "LED-only" intersection). The inverter shall provide an minimum active output capacity of 1500 Watts/2000 VA, with 80% minimum inverter efficiency.

13.3.2 The transfer time to switch from utility power to battery backed inverter power shall be 150 milliseconds maximum.

13.3.3 Optional: A user adjustable delay of the time from loss of utility power to power transfer, of from zero to five seconds should be provided.

13.3.4 When the utility line power has been restored at above 105 VAC ±2 VAC and below 125 VAC ±2VAC for 30 seconds, the BBS shall dropout of battery backup mode and return to utility line mode.

13.3.4.1 Optional: When the utility line power has been restored at above 105 VAC ±2 VAC and below 125 VAC ±2VAC for a user selected period of zero to 30 seconds, the BBS shall dropout of battery backup mode and return to utility line mode.

13.3.5 Utility Line Mode shall be Standby Mode.

13.3.5.1 Optional: Utility Line Mode may be user selected as either Standby Mode or Continuous Mode.

13.3.6 When in Standby Mode, utility line power is passed through the Transfer Relay to power the 332 Cabinet. The Inverter/Charger Unit recharges the batteries.

13.3.7 When in Continuous Mode, utility line power is passed through the Transfer Relay to the Inverter/Charger Unit. The Inverter/Charger Unit supplies conditioned AC power to the 332 Cabinet and recharges the batteries.

13.3.8 The BBS shall provide the user with 3-sets of normally open (NO) and normally closed (NC) single-pole double-throw (SPDT) relay contact closures, available on a panel-mounted terminal block, rated at a minimum 120V/1A, and labeled so as to identify each contact.

13.3.9 The first set(s) of NO and NC contact closures shall be energized whenever the unit switches to battery power. The contact shall be labeled or marked " On Batt."

13.3.10 The second set(s) of NO and NC contact closures shall be energized whenever the unit is running on battery power and the battery approaches approximately 40% of remaining useful capacity. The contact shell be labeled or marked "Low Batt."

13.3.11 The third set(s) of NO and NC contact closures shall be energized two hours after the unit switches to battery power. The contact shall be labeled or marked "Timer."

13.3.12 Operating temperature for both the inverter/power transfer relay and manual bypass switch shall be –37 º C to +74 º C.

13.3.13 Both the Power Transfer Relay and Manual Bypass Switch shall be rated at 240VAC/30 amps, minimum.

13.3.14 The BBS shall use a temperature-compensated battery charging system. The charging system shall compensate over a range of 2.5 to 4.0 mV/º C per cell.

13.3.15 The temperature sensor shall be external to the inverter/charger unit. The temperature sensor shall come with 2 meters (6'6") of wire.

13.3.16 Batteries shall not be recharged when battery temperature exceeds 40 º C ±3 º C.

13.3.17 The BBS shall bypass the utility line power whenever the utility line voltage is outside of the following voltage range: 100 VAC to 130 VAC (±2 VAC).

13.3.18 When utilizing battery power, the BBS output voltage shall be between 110 VAC and 125 VAC, pure sine wave output (less then 5% THD), 60 Hz ±3 Hz.

13.3.19 The BBS shall be compatible with Caltrans and LACO Underground Service Cabinets or Caltrans and LACO 332 Cabinets, with Model 170 Controllers, Model 2070 Controllers and cabinet components for full time operation.

13.3.20 BBS shall be equipped to prevent a malfunction feedback to the cabinet or from feeding back to the utility service.

13.3.21 In the event of inverter/charger failure, battery failure or complete battery discharge, the power transfer relay shall revert to the NC state, where utility line power is reconnected to the cabinet.

13.3.22 Recharge time for the battery, from "protective low-cutoff' to 80% or more of full battery charge capacity, shall not exceed twenty (20) hours.

Section 4 MOUNTING/ CONFIGURATION

13.4.1 **GENERAL**

13.4.1.1 Inverter/Charger Unit shall be rack mounted.

13.4.1.2 The Power Transfer Relay and Manual Bypass Switch shall be mounted in the same cabinet (Service Cabinet, the 332 Cabinet or the External Battery Cabinet) as the inverter/charger unit.

13.4.1.3 If mounted in a 332 Cabinet, the Power Transfer Relay and Manual Bypass Switch shall be mounted on the 332 Cabinet standard Electronic Industries Association (EIA) rail.

13.4.1.4 All provided wire for connecting between Power Transfer Relay, Bypass Switch and Cabinet Terminal Service Block shall be no less than 2 meters (6'6") of #10 AWG wire or longer if needed.

13.4.1.5 All provided wire for Relay contact wiring for each set of NO/NC relay contact closure terminals shall be no less than 2 meters (6'6") of #18 AWG wire or longer if needed.

13.4.1.6 See Figures 1, 3 and 4, which provides clarification as to how BBS Power Transfer Relay and Manual Bypass Switch are connected with Model 332A Cabinets in order to ensure interchangeability between all BBS manufacturers.

13.4.1.7 All necessary hardware for mounting (shelf angles, rack, etc) shall be provided. A minimum of 6 bolts/fasteners shall be used to secure swing-trays to the 332 Cabinet standard EIA 482.6mm (19") rack. All bolts/fasteners and washers shall meet the following requirements:

13.4.1.7.1 Screw type: Pan Head Phillips machine screw.

13.4.1.7.2 Size and Thread pitch: 10-32.

13.4.1.7.3 Material: 18-8 stainless steel (Type 316 stainless steel is acceptable as an alternate).

13.4.1.7.4 Washer: Use 1 flat washer (18-8 stainless steel) under the head of each 10-32 screw (provided that the screws are properly tightened, lock washers are unnecessary.).

13.4.1.7.5 Number of screws per swivel bracket, minimum: 6 screws (minimum) per swivel bracket. Spaced evenly along bracket, with one screw near each end.

13.4.2 UNDERGROUND SERVICE CABINET/BBS MOUNTING OPTION

13.4.2.1 THIS SHALL BE THE PREFERRED OPTION, WHEN POSSIBLE.

13.4.2.2 Refer to CHAPTER 1 Underground Service and Battery Back-Up System for New Traffic Signals, latest revision.

13.4.3 STANDALONE BBS CABINET OPTION

13.4.3.1 This should be used only where the underground service cabinet mounting option can not be used

13.4.3.2 The Batteries shall be housed in a NEMA 3R rated cabinet. The cabinet shall be mountable on a concrete pad. This Standalone BBS cabinet shall conform to LACO TSCES Chapter 6 Section 2 - Housings for the construction and finish of the cabinet.

13.4.3.3 The Pad mount base for concrete foundation shall be included with anchor bolts. Bolt hole pattern for mounting BBS cabinet to pad mount base shall be the same as for the Underground Service Pedestals, that is, 18.75 inch wide by 12.25 inch deep on center. See 14.1.3.3.2 below

13.4.3.4 The Inverter/Charger, Power Transfer Relay and manually operated Bypass Switch shall be mounted inside the Standalone BBS Cabinet.

13.4.3.5 Batteries shall be mounted on individual shelves.

13.4.3.6 A minimum of four shelves shall be provided.

13.4.3.7 Batteries may be installed upright or on their sides.

13.4.3.7.1 Upright Battery mounting: There shall be a minimum of 292.1 mm (11.5") clearance between shelves. Each shelf shall be a minimum of 203 mm (8.0 ") Deep X 393.7 mm (15.5" Wide.

13.4.3.7.2 Side Battery Mounting: There shall be a minimum of 216mm (8.5") clearance between shelves. Each shelf shall be a minimum of 292.1 mm (11.5") Deep X 393.7 mm (15.5" Wide).

13.4.3.8 Each shelf shall be capable of supporting a minimum of 57kg (125 lbs).

13.4.3.9 The Standalone BBS Cabinet shall be ventilated through the use of louvered vents (2), filters, and one thermostatically controlled fan as per Los Angeles County Traffic Signal Control Equipment Specifications (LACO TSCES) Chapter 6 Section 6.2.4 - Cabinet Housings, ventilation.

13.4.3.10 The Standalone BBS Cabinet shall have a door opening to the entire cabinet. The door shall be attached to the cabinet through the use of a continuous stainless steel or aluminum piano hinge. The door shall use a padlock clasp in order to lock the door.

13.4.3.11 The Standalone BBS Cabinet shall come with all bolts, conduits and bushings, gaskets, shelves, and hardware needed for mounting.

13.4.4 MODEL 332 CABINET, EXTERNAL BATTERY CABINET OPTION

13.4.4.1 This should be used only where the underground service cabinet mounting option cannot be used.

13.4.4.2 The Batteries shall be housed in a NEMA 3R rated cabinet. The cabinet shall be mountable on the side of the Model 332 Cabinet (see Figure 5 for details). This external battery cabinet shall conform to LACO TSCES Chapter 6 Section 2 - Housings for the construction and finish of the cabinet.

13.4.4.3 The Inverter/Charger, Power Transfer Relay and manually operated Bypass Switch shall be mounted inside the External Battery Cabinet.

13.4.4.4 Batteries shall be mounted on individual shelves.

13.4.4.5 A minimum of four shelves shall be provided.

13.4.4.6 Batteries may be installed upright or on their sides.

13.4.4.6.1 Upright Battery mounting: There shall be a minimum of 292.1 mm (11.5") clearance between shelves. Each shelf shall be a minimum of 203 mm (8.0 ") Deep X 393.7 mm (15.5" Wide.

13.4.4.6.2 Side Battery Mounting: There shall be a minimum of 216mm (8.5") clearance between shelves. Each shelf shall be a minimum of 292.1 mm (11.5") Deep X 393.7 mm (15.5" Wide).

13.4.4.7 Each shelf shall be capable of supporting a minimum of 57kg (125 lbs).

13.4.4.8 The External Battery Cabinet shall mount to the Model 332 Cabinet with a minimum of eight bolts. (See Figure 5)

13.4.4.9 The maximum dimensions of the external BBS/Battery Cabinet shall be as shown in Figure 13-5.

13.4.4.10 The External BBS/Battery Cabinet shall be ventilated through the use of louvered vents (2), filters, and one thermostatically controlled fan as per Los Angeles County Traffic Signal Control Equipment Specifications (LACO TSCES) Chapter 6 Section 6.2.4 - Cabinet Housings, ventilation.

13.4.4.11 The External BBS/Battery Cabinet shall have a door opening to the entire cabinet. The door shall be attached to the cabinet through the use of a continuous stainless steel or aluminum piano hinge. The door shall use a padlock clasp in order to lock the door

13.4.4.12 The External BBS/Battery Cabinet shall come with all bolts, conduits and bushings, gaskets, shelves, and hardware needed for mounting.

13.4.5 MODEL 332 CABINET, INTERNAL BATTERY OPTION

13.4.5.1 This should be used only where the underground service cabinet mounting option, the Standalone BBS Cabinet option or the external battery cabinet option cannot be used.

13.4.5.2 The BBS, including batteries, shall fit inside a typical, fully equipped Model 332 Cabinet that includes one Model 170 or 2070 controller.

13.4.5.3 The mounting method shall be rack-mount, swing-tray mount or combination of either. Front-mounted available rack space is 3U or approximately 152.4mm (6”). For additional space, see Figure 2 — BBS Mounting Diagram.

13.4.5.4 Batteries mounted below the controller shelf shall be swing-tray mounted. Batteries may be shelf mounted in area behind controller so long as shelf and batteries do not interfere with controller unit and C1 plug.

Section 5 BATTERY SYSTEM

13.5.1 Individual batteries shall be 12 Volt with a minimum rating of 65 Amp-Hour. The maximum weight shall not exceed 60 lb.

13.5.2 The Battery System shall consist of 4 to 8 batteries.

13.5.3 Batteries shall be deep cycle, sealed lead-acid based AGM/VRLA (Absorbed Glass Mat/ Valve Regulated Lead Acid).

13.5.4 Batteries shall be certified by the manufacturer to operate over a temperature range of - 40°C (-40°F) to +60°C (140°F).

13.5.5 The batteries shall be provided with appropriate connecting wiring and corrosion-resistant mounting trays and/or brackets appropriate for the cabinet into which they will be installed.

13.5.6 Batteries shall indicate maximum recharge data and recharging cycles.

13.5.7 Battery connecting wiring shall be via modular harness. Batteries shall be shipped with positive and negative terminals pre-wired with red and black cabling that terminates into a typical power-pole style connector. Harness shall be equipped with mating power-pole style connectors for batteries and a single, insulated plug-in style connection to inverter/charger unit. Harness shall allow batteries to be quickly and easily connected in any order and shall be keyed and wired to ensure proper polarity and circuit configuration.

13.5.8 Battery terminals shall be covered and insulated to prevent accidental shorting.

Section 6 MAINTENANCE, DISPLAYS, CONTROLS AND DIAGNOSTICS

13.6.1 The BBS shall include a display and/or meter to indicate current battery charge status and conditions.

13.6.2 The BBS shall have lightning surge protection compliant with LACO TSCES Chapter 1 GENERAL REQUIREMENTS, Section 9 ELECTRICAL, ENVIRONMENTAL, and TESTING (See CHAPTER 1Section 9 above).

13.6.3 The BBS shall be equipped with an integral system to prevent battery from destructive discharge and overcharge.

13.6.4 The BBS and batteries shall be easily replaced. Supplied with all needed hardware and shall not require any special tools for installation.

13.6.5 The BBS shall include a resettle front-panel event counter display to indicate the number of times the BBS was activated and a front-panel hour meter to display the total number of hours the unit has operated on battery power.

13.6.6 Manufacturer shall include two (2) sets of equipment lists, operation and maintenance manuals, and board-level schematic and wiring diagrams of the BBS, and the battery data sheets. Manuals shall conform to LACO, DPW TSCES (See **DOCUMENTATION**, section 1.3.4 above.

Section 7 WARRANTY

13.7.1 Manufacturers shall provide a two-year factory-repair warranty for parts and labor on the BBS from date of acceptance by the County. Batteries shall be warranted for full replacement for two (2) years from date of purchase. The warranty shall be included in the total bid price of the BBS.

13.7.2 Manufacturer shall provide Material Data Safety Sheets for potential hazardous substances.

Section 8 CHAPTER DETAILS

13.8.1 BATTERY BACKUP SYSTEM (BBS) BLOCK DIAGRAM:

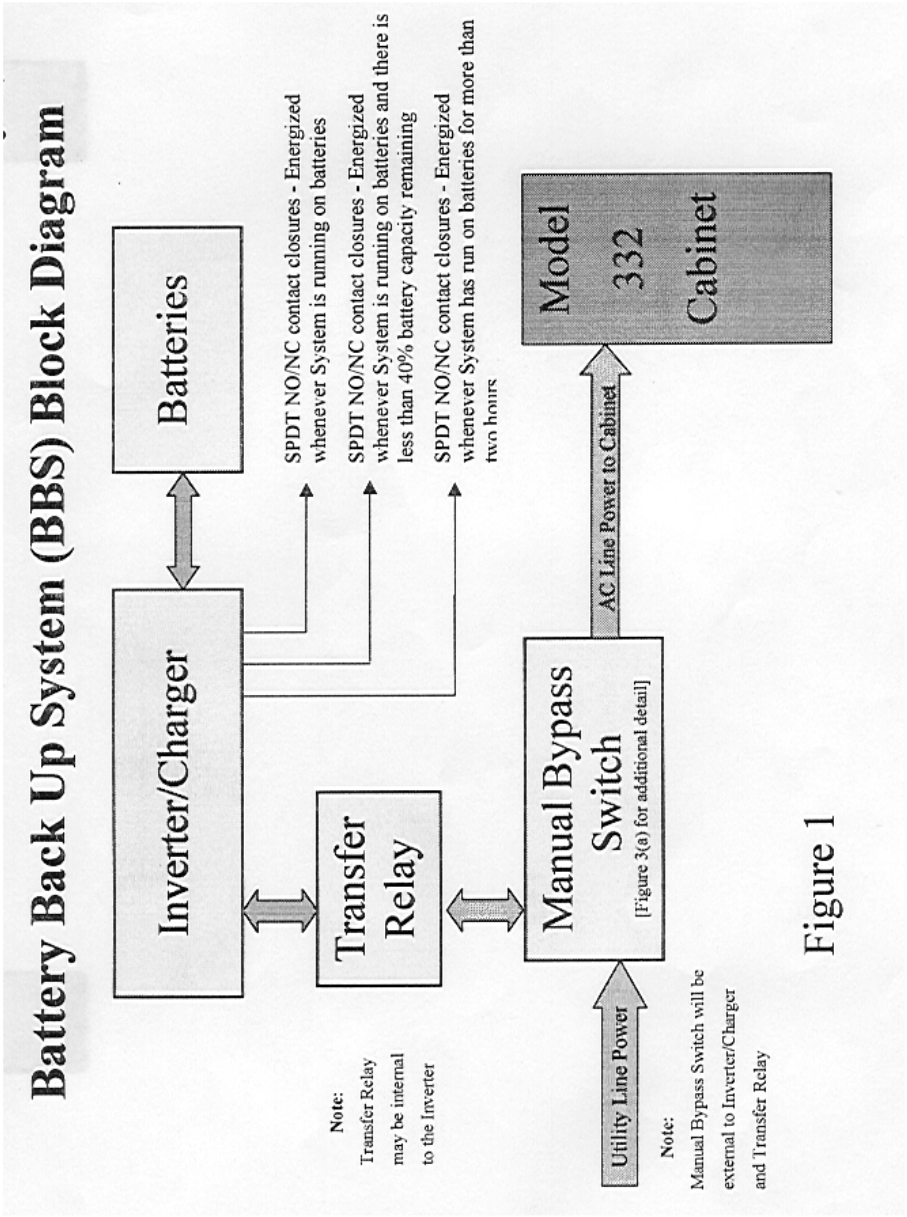


Figure 13-1: BBS BLOCK DIAGRAM

13.8.2 BBS MOUNTING DIAGRAM, UNDERGROUND SERVICE CABINET/BBS MOUNTING OPTION

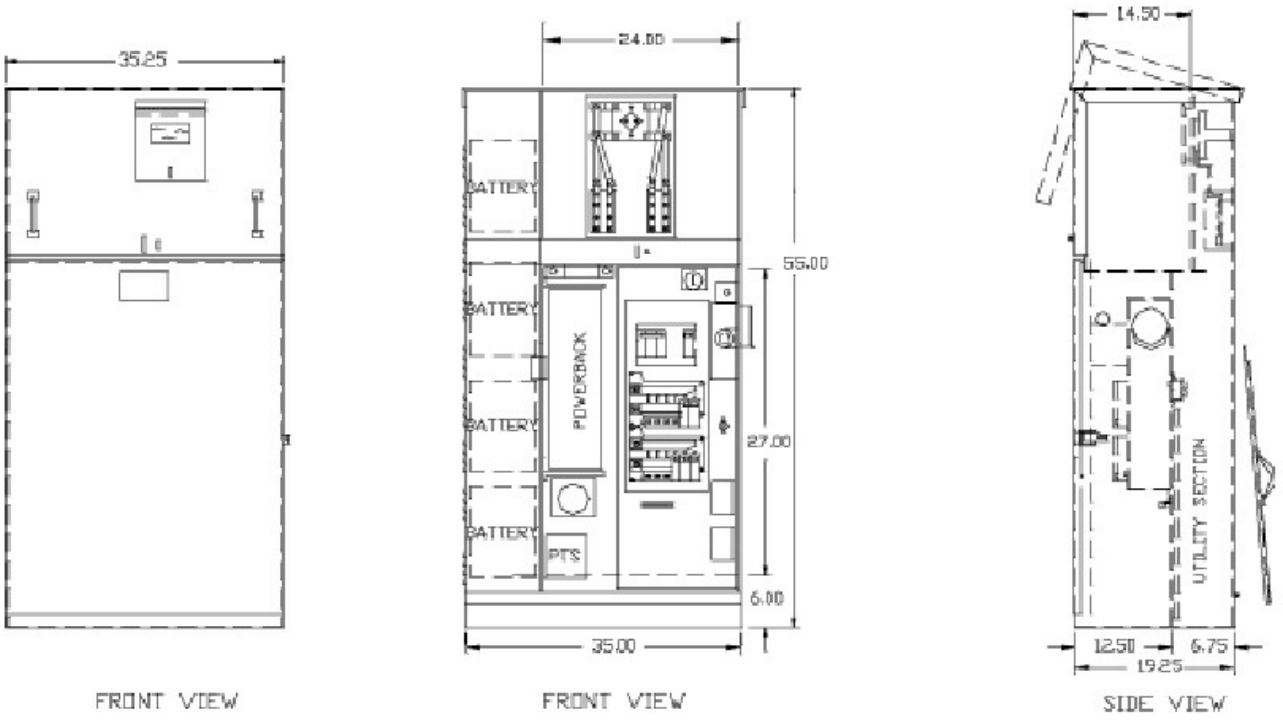


Figure 13-2: UNDERGROUND SERVICE/BBS CABINET.

13.8.3 BBS MOUNTING DIAGRAM, STANDALONE CABINET OPTION

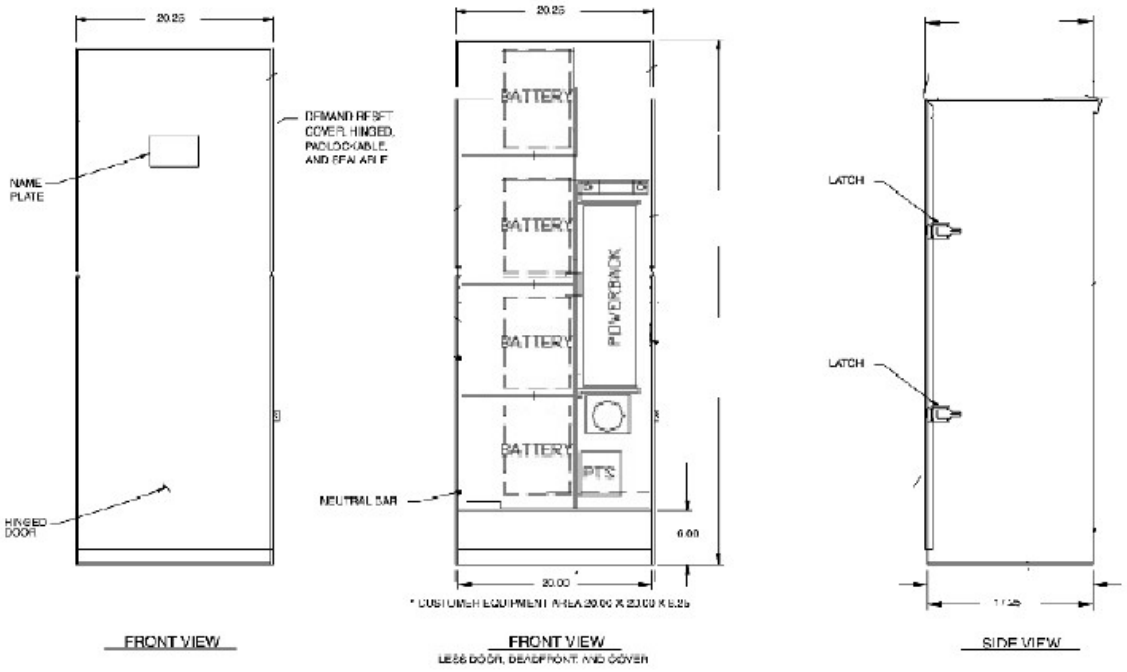


Figure 13-3: STANDALONE BBS CABINET

13.8.4 BBS MOUNTING DIAGRAM, INTERNAL BATTERY OPTION.

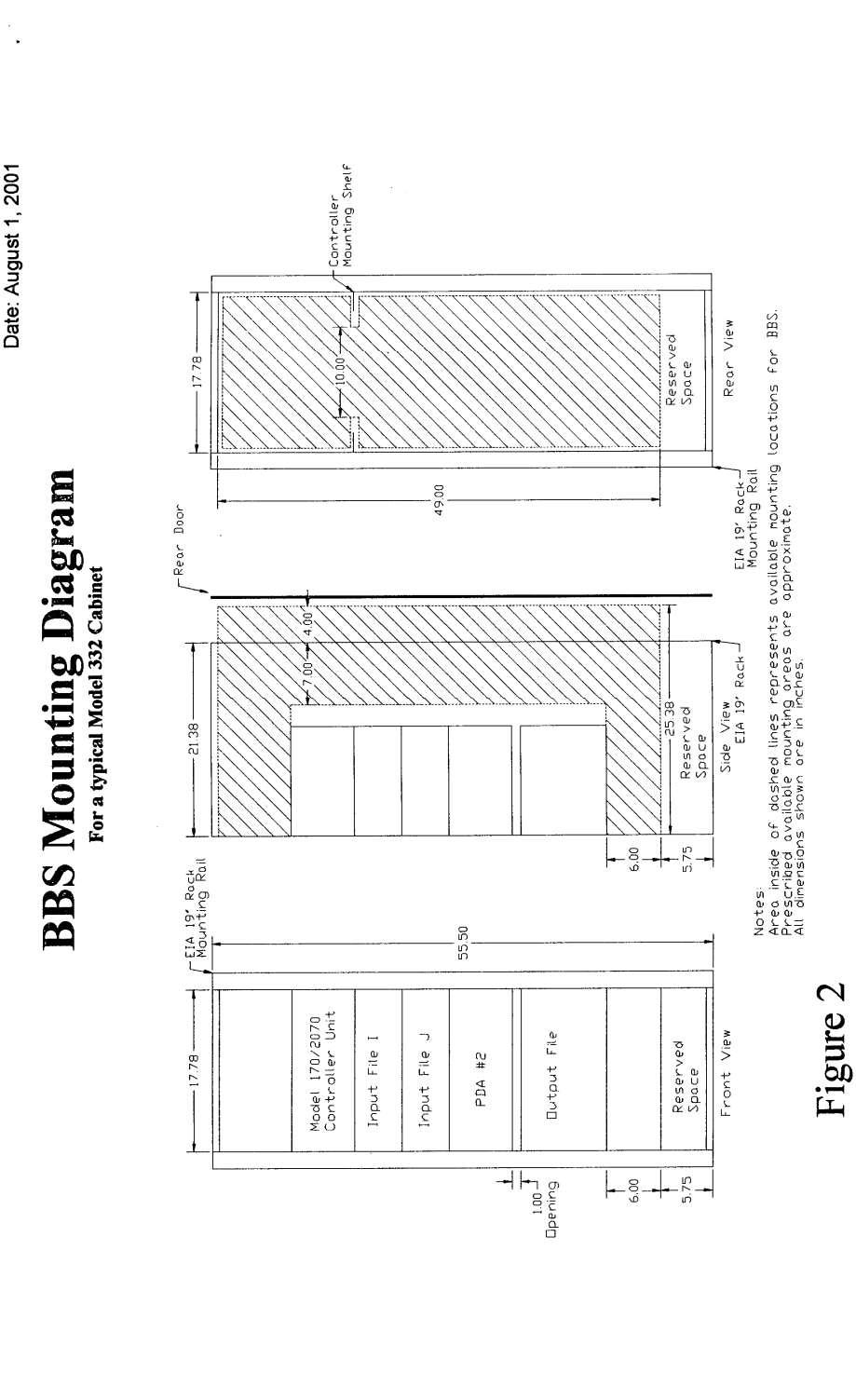
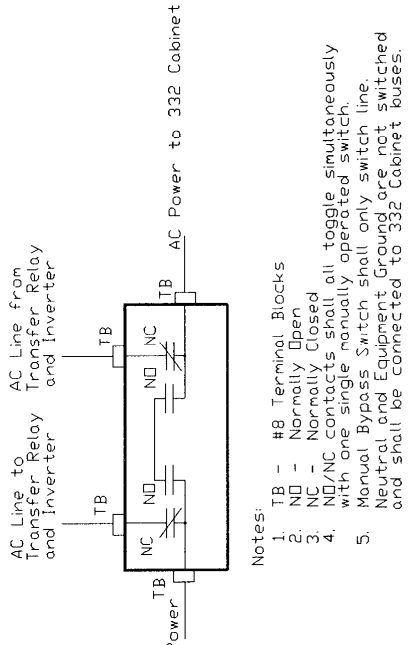


Figure 13-4: BBS MOUNTING DIAGRAM, 332 CABINET

BBS Specification Clarifications

(a) Manual Bypass Switch (typical)



Notes:
1. TB - #8 Terminal Blocks
2. NO - Normally Open
3. NC - Normally Closed
4. NO/NC contacts shall all toggle simultaneously with one single manually operated switch.
5. Manual Bypass Switch shall only switch line. Neutral and Equipment Ground are not switched and shall be connected to 332 Cabinet buses.

(b) Relay contacts (NO/NC) available on panel-mounted terminal block (typical)

Notes:
1. NO/NC contacts may either share or use separate commons.

Figure 3

Figure 13-5: MANUAL BYPASS SWITCH

BBS Utility Power Connection Diagram

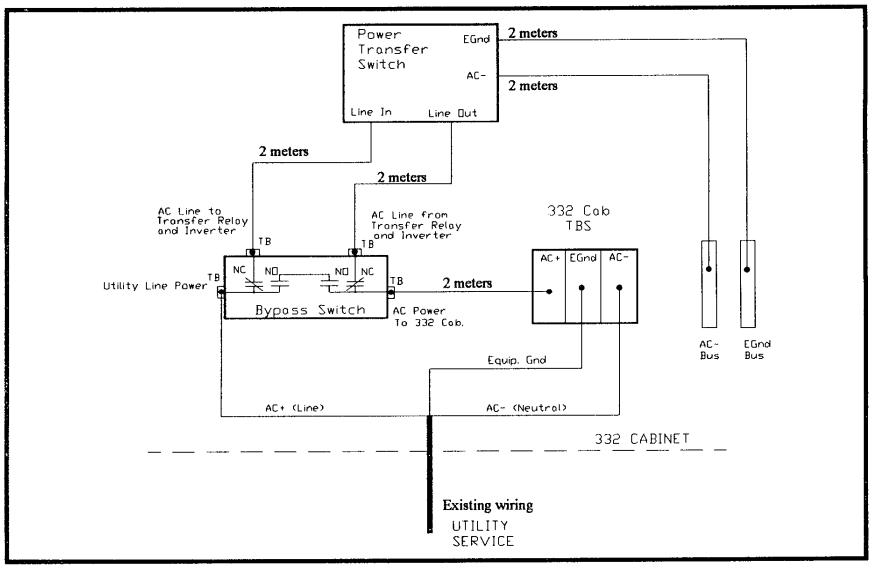


Figure 4

Figure 13-6: BBS UTILITY POWER CONNECTION DIAGRAM

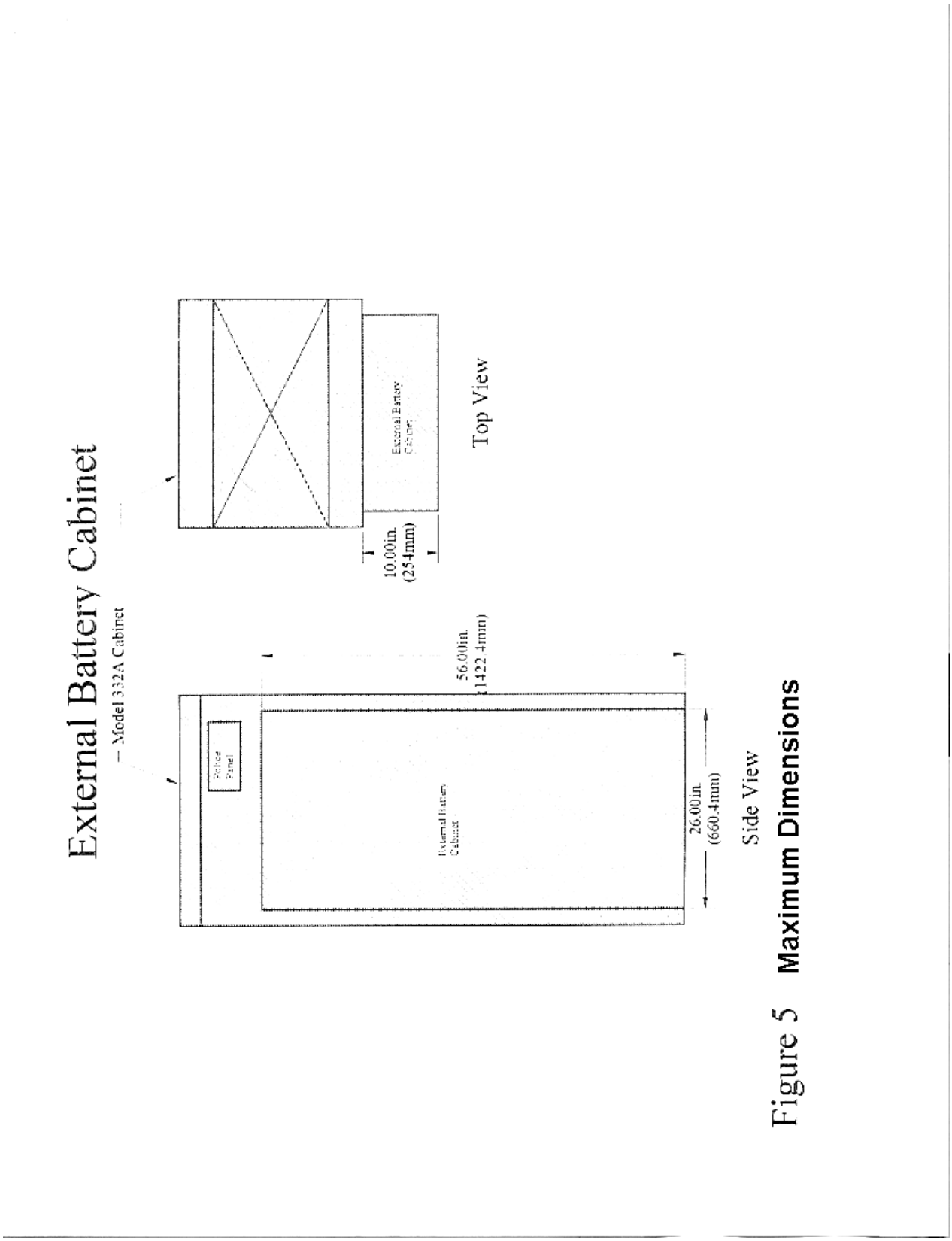


Figure 13-7: EXTERNAL BATTERY CABINET

CHAPTER 14 UNDERGROUND SERVICE PEDESTALS

Section 1 SCOPE

14.1.1 This specification establishes minimum standards for Underground Service Pedestals ("the unit") designed for use with Traffic Signal Controller Cabinets supplied to the County of Los Angeles.

14.1.2 The County remains the sole judge on the ability of each device to meet specifications.

14.1.3 **Enclosure**

14.1.3.1 The service unit shall comply with the current edition of the National Electrical Code.

14.1.3.2 Underwriter's Laboratories, Inc shall list the unit.

14.1.3.3 The unit shall comply with Cal Trans specifications ES2E except:

14.1.3.3.1 There shall be a separate independent main breaker for each buss set.

14.1.3.3.2 The bolt hole pattern for mounting service cabinet to pad mount base shall be 18.75 inch wide by 12.25 inch deep on center.

14.1.3.3.3 The Enclosure shall be 20.24 inch Wide by 17.25 inch Deep by 48 inch High.

14.1.3.3.4 The Customer section shall be 20 inch Wide by 10.5 inch Deep by 20 inch High.

14.1.3.4 The unit's enclosure shall be rainproof NEMA type 3R of anodized aluminum with minimum 0.125-inch wall thickness.

14.1.3.5 The unit shall meet requirements of EUSERC standard drawing number 308.

14.1.3.6 The unit shall be approved by; Los Angeles County Department of Public Works, California Department of Transportation, and Southern California Edison.

14.1.3.7 The unit's meter socket shall be 4 jaw, 100 amps, with test blocks.

14.1.3.8 The unit shall be standard voltage 120/240 volt, 1 phase, 3 wire.

14.1.3.9 The unit shall have 2 each, 6 circuit, tin-plated copper bussed interiors, one metered, the other unmetered.

14.1.3.10 The unit's bussed interiors will be configured to accommodate full size 120-volt single pole breakers for six (6) branch circuits.

14.1.3.11 The unit's utility landing lugs shall be rated for 200 amps.

14.1.3.12 The unit's enclosure shall have a utility test section.

14.1.3.13 All factory wiring shall be 600 volt rated copper.

14.1.3.14 The unit's enclosure shall be vandal-resistant and have hinged doors and dead fronts.

14.1.3.15 All hinged covers and doors will have full-length "piano" hinges.

14.1.3.15.1 All piano hinges shall be constructed of aluminum with stainless steel pins.

14.1.3.15.2 The method of attachment of the hinges shall be "plug welding".

14.1.3.16 The unit's utility doors and covers shall be sealable and padlockable.

14.1.3.17 The unit's Customer doors shall be padlockable.

14.1.3.18 The unit's Customer doors shall have a gasket to seal out moisture.

14.1.3.19 A pad mount base for concrete foundation, with anchor bolts, shall be included.

14.1.4 **Circuit Breakers**

14.1.4.1 The Metered main breaker shall be 2 pole, 120/240 volt, 100 amp, 10 KAIC, labeled "SERVICE DISC" and "METERED".

14.1.4.2 The Unmetered main breaker shall be 2 pole, 120/240 volt, 100 amp, 10 KAIC, labeled “SERVICE DISC” and “UNMETERED”.

14.1.4.3 All 120/240 volt 2 pole circuit breakers shall be common trip.

14.1.4.4 No tandem or split circuit breakers will be accepted.

14.1.4.5 The Metered buss shall be populated with the following breakers:

14.1.4.5.1 One each 50 amp, 1 pole, 120 volt, 10 KAIC, labeled “SIGNALS”.

14.1.4.5.2 One each 15 amp, 1 pole, 120 volt, 10 KAIC, labeled “SIGNS”.

14.1.4.6 The Unmetered buss shall be populated with the following breakers:

14.1.4.6.1 Two each 30 amp, 1 pole, 120 volt, 10 KAIC breakers each labeled “SAFETY LIGHTS”.

14.1.4.6.2 One each 15 amp, 1 pole, 120 volt, 10 KAIC, labeled “PE CONTROL”.

14.1.4.7 The copper bussed interiors will accept plug-in breakers manufactured by Bryant, GE, Westinghouse, ITE, Cutler-Hammer, and Crouse-Hinds/Murry.

Section 2 OPERATION AND MISCELLANEOUS INSTRUCTIONS

14.2.1 The Underground Service Pedestal shall have Two each PE cells and sockets with a test switch.

14.2.2 The PE test switch will have an “ON” and “AUTO” position.

14.2.3 The PE test switch will not have an “OFF” position.

14.2.4. A 2 pole or more, normally open, 35 amp or greater, lighting and heating control contactor with a 120-volt coil shall be provided for lighting. An equivalent, approved by Los Angeles County Department of Public Works, may be substituted. (Example: SIEMENS LEN00D003120A)

14.2.4 Each pole of the lighting contactor shall be fed separately by the “SAFETY LIGHT” breakers.

14.2.5 One PE cell socket shall be mounted so that the PE cell can be secured in the Utilities meter section.

14.2.6 This PE cell shall be fed by the “PE CONTROL” breaker and shall control the lighting contactor.

14.2.7 The test switch for this PE cell shall be in the Customer section and shall be labeled “SAFETY LIGHTS”.

14.2.8 The other PE cell socket shall be mounted so that the PE cell can be secured in the Customer section and be fed by the “SIGNS’ breaker. The test switch for this PE cell shall be in the Customer section and shall be labeled “SIGNS”.

14.2.9 The PE cell window or windows shall be covered with clear Lexan mounted to the inside of the enclosure.

14.2.10 The test switches shall be labeled “AUTO” and “ON” (or “TEST”) to indicate the corresponding position.

14.2.11 All labels shall be engraved and be of professional and durable quality. Labels shall be riveted in place.

14.2.12 A heavy duty, 600 volt RMS, six position barrier terminal strip (Marathon 1506STD, 1506DJ, or approved equivalent) shall be mounted in the lower part of the Customer section.

14.2.13 The load side of the lighting contactor shall be wired to the first two positions and the switched leg of the “SIGNS” PE cell shall be wired to the third position.

14.2.13.1 These terminals shall be labeled “SAFETY LIGHTS”, “SAFETY LIGHTS”, and “SIGNS” respectively.

14.2.14 The terminal screws shall be #10-32, nickel plated brass, standard machined slot binder head type (nether stamped nor a combination slot-Phillips), with screw inserts of the same material,

14.2.15 Base shall be general purpose phenolic, 150° C. There shall be 5/8-inch line-to-line spacing minimum.

14.2.16 Components in the Customer section shall be arranged to accommodate the addition of a second lighting contactor to be installed if necessary.

14.2.17 The neutral buss and the heavy duty barrier terminal strip shall be mounted below all other components including the space reserved to accommodate the optional second lighting contactor.

14.2.18 All components shall be new. The Los Angeles County Department of Public Works will not accept used, rebuilt, or refurbished components without prior approval.

14.2.19 Any deviation or exception to these specifications must be pre-approved by the Los Angeles County Department of Public Works.

Section 3 CHAPTER DETAILS

14.3.1 UNDERGROUND SERVICE PEDESTAL.

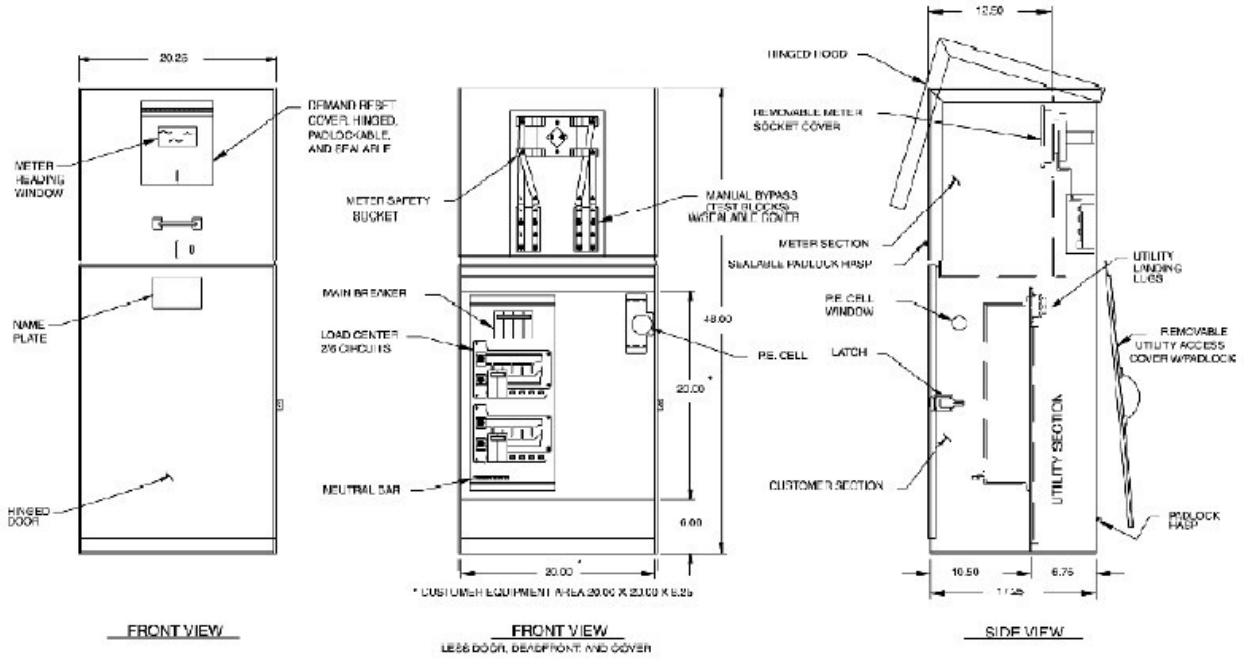


Figure 14-1: UNDERGROUND SERVICE PEDESTAL

CHAPTER 15 UNDERGROUND SERVICE AND BATTERY BACKUP SYSTEM FOR NEW TRAFFIC SIGNALS

Section 1 SCOPE

15.1.1 The following specifications establish minimum standards for battery back-up systems to be installed in conjunction with new underground electrical service cabinets.

Section 2 GENERAL

15.2.1 The underground electric service and the battery back-up system (BBS) shall be contained a in a single pedestal enclosure, constructed of anodized aluminum with a minimum of 0.125-inch wall thickness.

15.2.2 The enclosure shall be Dead Front construction, Vandal-resistant and Rainproof NEMA type 3R.

15.2.3 The enclosure shall also comply with the current edition of the National Electrical Code (NEC), National Electrical Manufacturer's Association (NEMA), Electric Utility Service Equipment Requirements Committee (EUSERC), Caltrans Transportation Electrical Equipment Specifications (TEES) and Los Angeles County Traffic Signal Control Equipment Specifications (LACO TSCES).

15.2.4 The underground service cabinet shall have metering compartment, underground utility, customer sections, and the BBS compartment. The equipment shall be listed by Underwriters Laboratories, Inc.

15.2.5 The Inverter/Charger, Power Transfer Relay and Manually Operated Bypass Switch shall be rack-mounted inside the Underground Service Cabinet.

15.2.6 Batteries shall be mounted on individual shelves with a minimum of four shelves inside the underground service cabinet. Each shelf shall have a minimum area of 228.6mm (9") X 431.8mm (17") in size, and shall have a minimum clearance of 292.1mm (11.5") between the shelves. Each shelf shall be capable of supporting a minimum of 57kg (125 lbs) . The compartment shall be ventilated through the use of louvered vents (2) with filters and one thermostatically controlled fan as per LACO TSCES requirements.

15.2.7 All hinged doors and covers shall use full-length "piano" hinges. The piano" hinges shall be constructed of aluminum with stainless steel pins. The door shall be attached to the hinge by "plug welding".

15.2.8 The hinge shall be attached to the cabinet with stainless-steel hardware.

15.2.9 Utility doors and covers shall be sealable and padlockable. Customer doors shall be padlockable.

15.2.10 Utility doors, Customer doors, and all covers shall be sealable with a gasket to seal out moisture.

15.2.11 Pad mount base for concrete foundation shall be included with anchor bolts. Bolt hole pattern for mounting service cabinet to pad mount base shall be 30.75 inch wide by 12.25 inch deep on center.

15.2.12 When viewed from the front, the Underground Service section shall be on the Right Half of the cabinet enclosure. *(Note: added for compatibility between different venders.)*

Section 3 ELECTRICAL

15.3.1 The meter socket shall be 4 jaw, 100 amps, 1-phase, 120/240 Volts and complete with test blocks. Utility landing shall be rated 200 amps. All wiring shall be copper and rated 600 volt.

15.3.2 The customer section shall have two sets of six-circuit load center with tin plated copper bus interiors for the metered and the unmetered loads. Load centers, the metered and the unmetered interior busses shall have their own 100 amps, 2-pole, 120/240 volt, and 10KAIC main circuit breakers.

15.3.3 The main 100 AMP circuit breakers shall be labeled “SERVICE DISC, METERED” and “SERVICE DISC, UNMETERED”.

15.3.4 The metered buss shall have the following branch circuit breakers:

15.3.4.1 One 50 amps, 1-pole, 120 volt, 10 KAIC, labeled “SIGNALS”.

15.3.4.2 One 15 amps, 1-pole, 120 Volt, 10 KAIC, labeled “ SIGNS”.

15.3.4.3 Four load centers shall be spare.

15.3.5 The unmetered buss shall have the following branch circuit breakers:

15.3.5.1 Two 30 amps, 1-pole, 120 volt, 10 KAIC breakers each labeled “SAFETY LIGHTS”.

15.3.5.2 One 15 amps, 1-pole, 120 volt, 10 KAIC, labeled “ PE CONTROL”.

15.3.5.3 Four load centers shall be spare. *(Note: added for clarity and to reflect current practice.)*

15.3.6 All 120/240 volt, 2-pole circuit breakers shall be of a common-trip type. No tandem or split circuit breakers will be accepted. Bryant, GE, Westinghouse/Cutler Hammer, and Crouse-Hinds/Murray manufacture acceptable plug-in circuit breakers.

15.3.7 The system shall have two PE cells and sockets with test switches for ON/AUTO positions; no “OFF” position is required. A 2 pole or more, normally open, 35 amp or greater, lighting and heating control contactor with a 120-volt coil shall be provided for lighting. An equivalent, approved by Los Angeles County Department of Public Works, may be substituted. (Example: SIEMENS LEN00D003120A) Each pole of the lighting contactor shall be fed separately by the “SAFETY LIGHT” circuit breaker.

15.3.8 One PE cell shall be secured in the in the utility metering compartment, fed by the “PE CONTROL” breaker, and control the mercury lighting contactor. The test switch of this PE cell shall be located in the customer section, labeled “SAFETY LIGHTS” and an “ON” and “AUTO” labels to indicate the corresponding position.

15.3.9 The other PE cell shall be secured in the customer section fed by the “SIGN” breaker. The test switch of this PE cell shall be located in the customer section and be labeled “SIGNS”, and a “ON” and “AUTO” labels to indicate the corresponding position.

15.3.10 The PE cell windows shall have a clear Lexan covers mounted to the inside of the enclosure.

15.3.11 A six-position barrier heavy-duty terminal strip, Marathon 1506 STD, 1506DJ, or approved equivalent, shall be provided and installed in the lower part of the customer section. The terminal screws shall be # 10-32, nickel-plated brass, standard machine slot binder head type, with screw inserts of the same material. Base shall be general-purpose phenolic, 150 degree C. There shall be a minimum of 5/8-inch line-to-line spacing. The terminal positions shall be labeled SIGNS, SIGNS, SAFETY LIGHTS, SAFETY LIGHTS, and SIGNS respectively.

15.3.12 Components in the customer section shall be arranged to accommodate future additional lighting contactor.

Section 4 BBS SYSTEMS

15.4.1 The Battery Back-up System (BBS) shall provide reliable emergency power to a traffic signal in the event of a power failure or interruption. That is, the BBS shall be capable of providing power for full run-time operation for an "LED-only" intersection (all colors, red, yellow, green and pedestrian indications) or flashing mode operation for an intersection using Red LED's.

15.4.2 The BBS shall include, but not be limited to the following: inverter/charger, power transfer relay, batteries, a separate manually operated non-electronic bypass switch and all necessary hardware and interconnect wiring.

15.4.3 The BBS shall provide a minimum of two (2) hours of full run-time operation for an "LED-only" intersection (at a minimum 700Watt / 1000VA load and provide a minimum active output capacity of 1500 Watts / 2000 VA, with 80% minimum inverter efficiency).

15.4.4 The maximum transfer time from loss of utility power to switchover to battery-backed inverter power shall be 150 milliseconds.

15.4.5 (Optional) The user shall be able to delay the power transfer time from zero to 5 seconds.

15.4.6 The BBS shall provide the user with 3-sets of normally open (NO) and normally closed (NC) single-pole double-throw (SPDT) relay contact closures, available on a panel-mounted terminal block, rated at a minimum 120V/1A, and labeled to identify each contact.

15.4.6.1 The first set of NO and NC contact closures shall be energized whenever the unit switches to battery power. The contact shall be labeled or marked "ON BATT."

15.4.6.2 The second set of NO and NC contact closures shall be energized whenever the battery approaches approximately 40% of remaining useful capacity. The contact shall be labeled or marked "LOW BATT."

15.4.6.3 The third set of NO and NC contact closures shall be energized two hours after the unit switches to battery power. The contact shall be labeled or marked "TIMER."

15.4.7 Operating temperature for both the inverter/power transfer relay and manual bypass switch shall be –37 º C to +74 º C.

15.4.8 Both the Power Transfer Relay and Manual Bypass Switch shall be rated at 240VAC/30 amps, minimum.

15.4.9 The BBS shall use a temperature-compensated battery charging system. The charging system shall compensate over a range of 2.5 to 4.0 mV/º C per cell.

15.4.10 The temperature sensor shall be external to the inverter/charger unit. The temperature sensor shall come with 2 meters (6'6") of wire.

15.4.11 Batteries shall not be recharged when battery temperature exceeds 50 º C ±3 º C.

15.4.12 The BBS shall bypass the utility line power whenever the utility line voltage is outside of the following voltage range: 100 VAC to 130 VAC (±2 VAC).

15.4.13 When utilizing battery power, the BBS output voltage shall be between 110 VAC and 125 VAC, pure sine wave output (less then 5% THD), 60 Hz ±3 Hz.

15.4.14 The BBS shall be compatible with Caltrans and LACO 332 Cabinets, Model 170 Controllers, Model 2070 Controllers and cabinet components for full time operation.

15.4.15 When the utility line power has been restored at above 105 VAC ±2 VAC and below 125 VAC ±2VAC for a user-selected period of zero to 30 seconds, the BBS shall dropout of battery backup mode and return to utility line mode.

15.4.16 BBS shall be equipped to prevent a malfunction feedback to the cabinet or from feeding back to the utility service.

15.4.17 In the event of inverter/charger failure, battery failure or complete battery discharge, the power transfer relay shall revert to the NC State, where utility line power is reconnected to the cabinet.

15.4.18 Recharge time for the battery, from “protective low-cutoff’ to 80% or more of full battery charge capacity, shall not exceed twenty (20) hours.

Section 5 MAINTENANCE, DISPLAYS, CONTROLS AND DIAGNOSTICS

15.5.1 The BBS shall include a display and/or meter to indicate current battery charge status and conditions.

15.5.2 The BBS shall have lightning surge protection compliant with LACO TSCES requirements.

15.5.3 The BBS shall be equipped with an integral system to prevent battery from destructive discharge and overcharge.

15.5.4 The BBS and batteries shall be easily replaced and shall not require any special tools for installation.

15.5.5 The BBS shall include a resetable front-panel event counter display to indicate the number of times the BBS was activated and a front-panel hour meter to display the total number of hours the unit has operated on battery power.

15.5.6 Manufacturers shall include two (2) sets of equipment lists, operation and maintenance manuals, and board-level schematic and wiring diagrams of the BBS, and the battery data sheets. Manual shall conform to Section 1.3.4.DOCUMENTATION

Section 6 BATTERY SYSTEM

15.6.1 Individual batteries shall be 12V type, 65 amp-hour rated. Maximum weight shall not exceed 60 lb., and shall be easily replaced and commercially available off the shelf.

15.6.2 The battery shall be mounted on individual shelves inside the battery compartment attached to the service cabinet and shall provide a minimum of 2 (two) hours normal operation and then revert to flash mode operation for 6 (six) hours or more.

15.6.3 Batteries used for BBS shall consist of 4 to 8 batteries

15.6.4 Batteries shall be deep cycle, sealed prismatic lead-calcium based AGM/VRLA (Absorbed Glass Mat/ Valve Regulated Lead Acid).

15.6.5 Batteries shall be certified by the manufacturer to operate over a temperature range of - 40°C (-40°F) to +60°C (140°F).

15.6.6 The batteries shall be provided with appropriate interconnect wiring and corrosion-resistant mounting trays and/or brackets appropriate for the cabinet into which they will be installed.

15.6.7 Batteries shall indicate maximum recharge data and recharging cycles.

15.6.8 Battery interconnect wiring shall be via modular harness. Batteries shall be shipped with positive and negative terminals pre-wired with red and black cabling that terminates into a typical power-pole style connector. Harness shall be equipped with mating power-pole style connectors for batteries and a single, insulated plug-in style connection to inverter/charger unit. Harness shall allow batteries to be quickly and easily connected in any order and shall be keyed and wired to ensure proper polarity and circuit configuration.

15.6.9 Battery terminals shall be covered and insulated so as to prevent accidental shorting.

Section 7 WARRANTY

15.7.1 Manufacturers shall provide a two (2) year factory-repair warranty for parts and labor on the BBS from date of acceptance by the County. Batteries shall be warranted for full replacement for two (2) years from date of purchase. The warranty shall be included in the total bid price of the BBS.

15.7.2 Manufacturers shall include Material Data Safety Sheets for potentially hazardous materials.

15.7.3 The BBS shall meet the minimum latest edition of CALTRANS BBS Specifications requirements. Tested, approved and in the Caltrans' Approved Product List (APL).

Section 8 CHAPTER DETAILS

15.8.1 UNDERGROUND SERVICE AND BATTERY BACKUP CABINET.

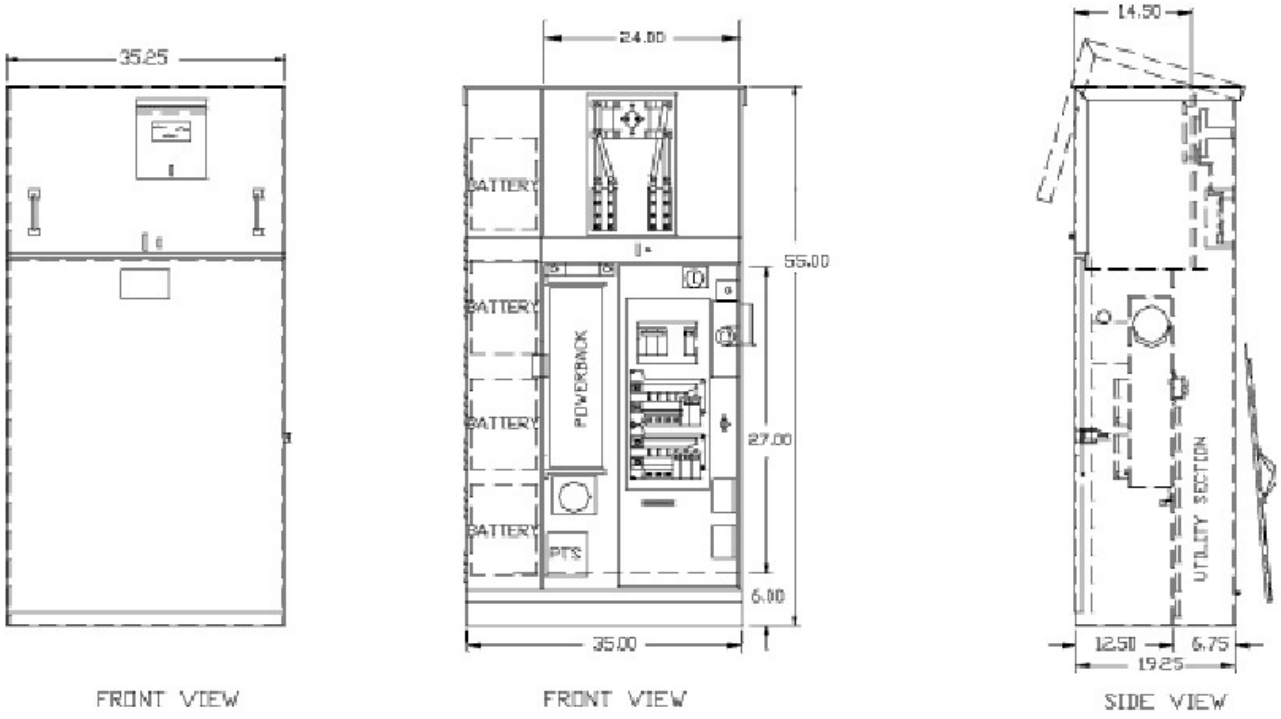


Figure 15-1: UNDERGROUND SERVICE AND BATTERY BACKUP SYSTEM

CHAPTER 16 LIGHT EMITTING DIODE (LED) SIGNAL MODULES

Section 1 SCOPE

16.1.1 This specification is for the purchase of light emitting diode (LED) Traffic Signal Modules (herein referred to as modules) in the following configurations: the 300 mm circular sections, the 200 mm circular sections, the 300 mm arrow sections, bicycle sections, programmable visibility sections, and lane control sections. All devices must meet the general specifications of the Transportation Electrical Equipment Specifications (TEES), Chapter 1--General Specifications, as well as the following specification. In case of conflict, this specification shall govern over the TEES, Chapter 1.

Section 2 GENERAL

16.2.1 Each module shall consist of an assembly that utilizes LED's as the light source in lieu of an incandescent lamp for use in traffic signal sections.

16.2.2 The LED's utilized in the modules shall be AlInGaP technology for red, amber and yellow indications, or GaN for green indications, and shall be the ultra bright type rated for 100,000 hours of continuous operation from - 40°C to +74°C.

16.2.3 The modules shall be rated for a minimum useful life of 48 months. All modules shall meet all parameters of this specification during this period.

16.2.4 The individual LED's shall be wired such that a catastrophic loss or the failure of one or more LED will not result in the loss of the entire module.

16.2.5 Electrical

16.2.5.1 Power Consumption

16.2.5.2 Maximum power consumption for LED modules is per Table 2-1.

16.2.5.3 LED modules will have EPA Energy Star compliance ratings, if applicable to that shape, size and color.

16.2.5.4 Operating Voltage

16.2.5.4.1 Operating voltage of the modules shall be from a 60 HZ ±3 HZ AC line over a voltage ranging from 95 volts to 135 volts. The fluctuations of line voltage shall have no visible effect on the luminous intensity of the indications.

16.2.5.5 Power Factor: The LED signal module shall have a power factor of 0.90 or greater.

16.2.5.6 THD: Total harmonic distortion (current and voltage) induced into an AC power line by a LED signal module shall not exceed 20 percent

16.2.5.7 Surge Suppression: The signal module on-board circuitry shall include voltage surge protection to withstand high-repetition noise transients as stated in Section 2.1.6 of NEMA Standard TS-2, 1992. Publication: Equipment and Material Standards, Chapter 2 (Vehicle Traffic Control Signal Heads).

16.2.5.8 The LED circuitry shall prevent perceptible flicker to the unaided eye over the voltage range specified above.

16.2.5.9 All wiring and terminal blocks shall meet the requirements of Section 13.02 of the ITE Publication: Equipment and Material Standards, Chapter 2 (Vehicle Traffic Control Signal Heads).

16.2.5.10 Compatibility: The modules shall be operationally compatible with currently used controller assemblies (solid state load switches, flashers, and conflict monitors). Review Chapters CHAPTER 4, CHAPTER 5 and CHAPTER 12 specifications for these devices.

16.2.5.11 When a current of 20 mA AC (or less) is applied to the unit, the voltage read across the two leads shall be 15 VAC or less.

16.2.5.12 The modules and associated on-board circuitry must meet Class A emission limits referred in Federal Communications Commission (FCC) Title 47, Subpart B, Section 15 regulations concerning the emission of electronic noise.

16.2.6 Photometric Requirements

16.2.6.1 The minimum initial luminous intensity values for the modules shall be as stated in Table 2-2 and/or Table 2-4 at 25°C.

16.2.6.2 The modules (excluding yellow) shall meet or exceed the illumination values as shown in Table 2-3 and/or Table 2-5, throughout the useful life based on normal use in a traffic signal operation over the operating temperature range.

16.2.6.3 Yellow modules shall meet or exceed the illumination values as shown in Table 2-3 and/or Table 2-5, throughout the useful life based on normal use in a traffic signal operation at 25°C.

16.2.6.4 The measured chromaticity coordinates of the modules shall conform to the chromaticity requirements of Table 2-6, throughout the useful life over the operating temperature range.

16.2.7 Physical and Mechanical Requirements: LED traffic signal modules shall be designed as retrofit replacements for existing optical units of signal indications and shall not require special tools for installation. See appropriate sections for Type 1 and Type 2 modules.

16.2.8 Environmental Requirements

16.2.8.1 The LED signal module shall be rated for use in the operating temperature range of: - 40°C (- 40°F) to +74°C (+165°F). The modules shall meet all specifications throughout this range.

16.2.8.2 The LED signal module shall be protected against dust and moisture intrusion per the requirements of NEMA Standard 250-1991 for Type 4 enclosures to protect all internal components.

16.2.9 Construction

16.2.9.1 The LED signal module shall be a single, self-contained device, not requiring on-site assembly for installation into an existing traffic signal housing. The power supply for the module shall be integral to the unit.

16.2.9.2 The circuit board and power supply shall be contained inside the module. Circuit boards shall conform to section 1.7.1. of these equipment specifications".

16.2.9.3 The assembly and manufacturing process for the LED signal assembly shall be designed to assure all internal components are adequately supported to withstand mechanical shock and vibration from high winds and other sources.

16.2.10 Materials

16.2.10.1 Material used for the lens and signal module construction shall conform to ASTM specifications for the materials.

16.2.10.2 Enclosures containing the power supply and/or electronic components of the signal module shall be made of UL94VO flame retardant materials. The lens of the signal module is excluded from this requirement.

16.2.11 Module Identification

16.2.11.1 Each module shall have the manufacturer's name, trademark, model number, serial number, date of manufacture (month-year), and lot number as identification permanently marked on the back of the module.

16.2.11.2 The following operating characteristics shall be permanently marked on the back of the module: rated voltage and rated power in Watts and Volt-Ampere.

16.2.11.3 Each module shall have a symbol of the type of module (i.e. circle, arrow, etc.) in the color of the module. The symbol shall be one inch (25.4 mm) in diameter. Additionally, the color shall be written out in ½ in letters next to the symbol.

16.2.11.4 If a specific mounting orientation is required, each module shall have prominent and permanent marking(s) for correct indexing and orientation within a signal housing. The markings shall consist of an up arrow, or the word "UP" or "TOP".

Section 3 TYPE 1 TRAFFIC SIGNAL MODULE

16.3.1 The following specification requirements apply to the Type 1 module only. All general specifications apply unless specifically superceded in this section.

16.3.2 Type 1 modules can be manufactured under this specification for the following faces:

16.3.2.1 300 mm circular

16.3.2.2 200 mm circular

16.3.2.3 300 mm arrow

16.3.2.4 Bicycle indication (future)

16.3.2.5 Lane Control (future)

16.3.3 **Physical and Mechanical Requirements**

16.3.3.1 The module shall fit into existing traffic signal section housings built to the specifications detailed in ITE Publication: Equipment and Material Standards, Chapter2 (Vehicle Traffic Control Signal Heads).

16.3.3.2 Each Type 1 module shall be designed to be installed in the doorframe of a standard traffic signal housing. The Type 1 module shall be sealed in the doorframe with a one-piece EPDM (ethylene propylene rubber) gasket.

16.3.3.3 The maximum weight of a Type 1 module shall be 1.8 kg (4 lbs.).

16.3.3.4 Each Type 1 module shall be a sealed unit to include all parts necessary for operation (a printed circuit board, power supply, a lens and gasket, etc.), and shall be weather proof after installation and connection.

16.3.3.5 Conductors : Two secured, color coded, 600 V, 20 AWG minimum, jacketed wires, conforming to the National Electric Code, rated for service at +105°C, are to be provided for electrical connection for each Type 1 LED signal module. Conductors for Type 1 modules shall be 1-m in length, with quick disconnect terminals attached and shall conform to Section 86-4.01C, "Electrical Components," of the Standard Specifications.

16.3.3.6 If specified in the purchased order, the module will be equipped with an adapter that will screw into the medium base, lamp socket. The adapter shall be able to accept the quick disconnect terminals at the end of the conductors for the module. The electrical contacts of the adapter shall be made of brass.

16.3.4 **Lens**

16.3.4.1 The lens of the Type 1 module shall be integral to the unit, shall be convex with a smooth outer surface and made of plastic or of glass.

16.3.4.2 The lens shall be tinted to enhance ON/OFF contrast.

16.3.4.3 The use of tinting or other materials to enhance ON/OFF contrasts shall not affect chromaticity and shall be uniform across the face of the lens.

16.3.4.4 The LED signal module lens shall be UV stabilized and shall be capable of withstanding ultraviolet (direct sunlight) exposure for a minimum period of 60 months without exhibiting evidence of deterioration.

16.3.4.5 If a polymeric lens is used, a surface coating or chemical surface treatment shall be used to provide front surface abrasion resistance.

Section 4 TYPE 2 TRAFFIC SIGNAL MODULE

16.4.1 The following specification requirements apply to the Type 2 module only. All general specifications apply unless specifically superceded in this section.

16.4.2 Type 2 modules can be manufactured under this specification for the following faces:

16.4.2.1 300 mm circular

16.4.2.2 200 mm circular

16.4.2.3 300 mm arrow

16.4.2.4 Programmed Visibility (red, yellow, green)

16.4.3 **Physical and Mechanical Requirements**

16.4.3.1 The module shall fit into existing traffic signal section housings built to the specifications detailed in the ITE Publication: Equipment and Material Standards, Chapter 2 (Vehicle Traffic Control Signal Heads), with the existing lens, reflector and lamp socket remaining in place, and without modification to the housing.

16.4.3.2 Each Type 2 module shall be designed to mount in the standard lamp socket normally used with an incandescent lamp.

16.4.3.3 The maximum weight of a Type 2 module shall be 1.4 kg (3 lbs.).

16.4.3.4 Type 2 modules shall be a sealed unit containing all components necessary for operation.

16.4.3.5 The installation of a Type 2 module shall not require any removal of, or modification to the standard lamp socket or reflector. The installation of a Type 2 module shall not require special tools.

Section 5 300 MM ARROW

16.5.1 The following specification requirements apply to the 300 mm arrow module only. All general specifications apply unless specifically superceded in this section.

16.5.2 The arrow module shall meet specifications stated in Section 9.01 of the ITE Publication: Equipment and Material Standards, Chapter 2 (Vehicle Traffic Control Signal Heads) for arrow indications.

16.5.3 The LED's shall be spread evenly across the illuminated portion of the arrow area.

Section 6 300 MM BICYCLE

16.6.1 The following specification requirements apply to the 300 mm bicycle module only. All general specifications apply unless specifically superceded in this section.

16.6.2 The bicycle module shall approximate shape and size specifications as shown in Figure 6-1 for bicycle signal face. Caltrans shall make the final determination as to the conformance to the intent of the specification.

16.6.3 The LED's shall be spread evenly across the illuminated portion of the bicycle area.

Section 7 300 MM PROGRAMMED VISIBILITY (PV)

16.7.1 The following specification requirements apply to the 300 mm PV module only. All general specifications apply unless specifically superceded in this section.

16.7.2 The module shall be a Type 2 module designed and constructed to be installed in a programmed visibility (PV) signal housing with out modification to the housing.

16.7.3 The LED's shall be spread evenly across the illuminated portion of the bicycle area.

Section 8 300 MM LANE CONTROL

16.8.1 The following specification requirements apply to the 300 mm lane control module only. The lane control module is a single, combination module with both a red X and green arrow. All general specifications apply unless specifically superceded in this section.

16.8.2 The lane control module shall approximate shape and size specifications as shown in Figures 8-1 and 8-2 for lane control modules. Caltrans shall make the final determination as to the conformance to the intent of the specification.

16.8.3 The LED's shall be spread evenly across the illuminated portion of the bicycle area.

16.8.3.1.1 **300 mm Lane Control**

16.8.4 The following specification requirements apply to the 300 mm lane control module only. The lane control module is a single, combination module with both a red X and green arrow. All general specifications apply unless specifically superceded in this section.

16.8.5 The lane control module shall approximate shape and size specifications as shown in Figures 8-1 and 8-2 for lane control modules. Caltrans shall make the final determination as to the conformance to the intent of the specification.

16.8.6 Three secured, color coded, 600 V, 20 AWG minimum, jacketed wires, conforming to the National Electric Code, rated for service at +105°C, are to be provided for electrical connection for each lane control LED signal module. Conductors for this module shall be 1-m in length, with quick disconnect terminals attached and shall conform to Section 86-4.01C, "Electrical Components," of the Standard Specifications. The color code is as follows:

Function	Color
neutral	white
red X	red
green arrow	brown

16.8.7 The LED's shall be spread evenly across the illuminated portions of this module.

Section 9 QUALITY ASSURANCE

16.9.1 The modules shall be manufactured in accordance with a manufacturer quality assurance (QA) program. The QA program shall include two types of quality assurance: (1) design quality assurance and (2) production quality assurance. The production quality assurance shall include statistically controlled routine tests to ensure minimum performance levels of LED signal modules built to meet this specification, and a documented process of how problems are to be resolved.

16.9.2 QA process and test results documentation shall be kept on file for a minimum period of seven years.

16.9.3 LED signal module designs not satisfying design qualification testing and the production quality assurance testing performance requirements described below shall not be labeled, advertised, or sold as conforming to this specification.

16.9.4 **Design Qualification Testing**

16.9.4.1 Design Qualification Testing shall be performed by the manufacturer or an independent testing lab hired by the manufacturer on new LED module designs, and when a major design change has been implemented on an existing design.

16.9.4.2 A major design change is defined as a design change (electrical or physical) which changes any of the performance characteristics of the module, results in a different circuit configuration for the power supply, or changes the layout of the individual LED's in the module.

16.9.4.3 A quantity of two units for each design shall be submitted for Design Qualification Testing.

16.9.4.4 Test units shall be submitted to County of Los Angeles, Department of Public Works, Traffic Signal Lab after the manufacturer's testing is complete.

16.9.4.5 Manufacturer's testing data shall be submitted with test units for County verification of Design Qualification Testing data.

16.9.4.6 Burn In: The sample modules shall be energized for a minimum of 24 hours, at 100 percent on-time duty cycle, at a temperature of +74°C (+165°F), before performing any design qualification testing.

16.9.4.7 Any failure of the module, which renders the unit non-compliant with the specification after burn-in, shall be cause for rejection.

16.9.4.8 For Design Qualification Testing, all specifications will be measured including, but not limited to:

16.9.4.9 Rated Initial Luminous Intensity measured at +25°C.

16.9.4.10 Chromaticity (Color), measured at +25°C.

16.9.4.11 Electrical: All specified parameters shall be measured and used for quality comparison of production quality assurance on production modules (rated power, etc).

16.9.4.12 Equipment Compatibility: Modules shall be tested for compatibility with the controller unit, conflict monitor, and load switch. Each signal module shall be connected to the output of a standard load switch connected to an AC voltage supply between the values of 95 and 135 VAC, with the input to the load switch in the "off" position. The AC voltage developed across each LED signal module so connected shall not exceed 10 Vrms as the input AC voltage is varied from 95 Vrms to 135 Vrms.

16.9.4.13 Mechanical vibration testing shall be as per MIL-STD-883, Test Method 2007, using 3 four minute cycles along each x, y, and z axis, at a force of 2.5 Gs, with a frequency sweep from 2 HZ to 120 HZ. The loosening of the lens, or of any internal components, or other physical damage shall be cause for rejection.

16.9.4.14 Temperature cycling shall be performed as per MIL-STD-883, Test method 1010. The temperature range shall be per "Environmental Requirements". A minimum of 20 cycles shall be performed with a 30 minute transfer time between temperature extremes and a 30 minute dwell time at each temperature. Module (s) being tested shall be energized and functioning throughout the duration of the test. Failure of a module to function properly or any evidence of cracking of the module lens or housing after temperature cycling shall be cause for rejection.

16.9.5 **Production Quality Control Testing.**

16.9.5.1 The following Production Quality Assurance tests shall be performed on each new module prior to shipment. Failure to meet requirements of any of these tests shall be cause for rejection. Test results shall be retained by the manufacturer for seven years.

16.9.5.2 Burn-in period shall consist of each signal module being energized at rated voltage for a 30-minute stabilization period before the measurement is made (except for yellow modules).

16.9.5.3 Each module shall be tested for rated initial intensity after burn-in.

16.9.5.4 A single point measurement, with a correlation to the intensity requirements of Table 2-2 for circular modules, may be used.

16.9.5.5 The ambient temperature for this measurement shall be +25°C (+77°F).

16.9.5.6 Each module not meeting minimum luminous intensity requirements per Table 2-2 or Table 2-4 shall be cause for rejection.

16.9.5.7 Each module shall be tested for required power factor after burn-in.

16.9.5.8 Each module shall be measured for current flow in amperes after burn-in. The measured current values shall be compared against rated values resulting from design qualification measurements under "Design Qualification Testing". The current flow shall not exceed the rated value.

16.9.5.9 Each module shall be visually inspected for any exterior physical damage or assembly anomalies. Careful attention shall be paid to the surface of the lens to ensure there are no scratches (abrasions), cracks, chips, discoloration, or other defects. Any such defect shall be cause for rejection.

16.9.6 **County Quality Assurance Testing.**

16.9.6.1 The County may perform testing on all shipments.

16.9.6.2 Testing should be completed within 30 days after delivery to the specified location the purchase order.

16.9.6.3 All parameters of the specification may be tested on the shipment sample.

Section 10 WARRANTY

16.10.1 In addition to meeting the performance requirements for the minimum period of 48 months, the manufacturer shall provide a written warranty against defects in materials and workmanship for the modules for a period of 60 months after acceptance of the modules. Replacement modules shall be provided promptly after receipt of modules that have failed at no cost to the County. All warranty documentation shall be given to the Traffic Signal Lab prior to ~~random sample~~ testing.

Section 11 TABLES

16.11.1 Maximum Power Consumption (in Watts)

	Red		Yellow		Green	
Temperature	25°C	74°C	25°C	74°C	25°C	74°C
300 mm circular	11	17	22	25	15	15
200 mm circular	8	13	13	16	12	12
300 mm arrow	9	12	10	12	11	11
Bicycle indication	11	17	22	25	15	15
PV indication	11	17	22	25	15	15
Lane Control (X)	9	12	n/a	n/a	n/a	n/a
Lane Control (Arrow)	n/a	n/a	n/a	n/a	11	11

Figure 16-1: MAXIMUM POWER CONSUMPTION

16.11.2 Minimum Initial Intensities for Circular Indications (in cd)

	200 mm			300 mm		
Angle (v, h)	Red	Yellow	Green	Red	Yellow	Green
2.5, ±2.5	157	314	314	399	798	798
2.5, ±7.5	114	228	228	295	589	589
2.5, ±12.5	67	133	133	166	333	333
2.5, ±17.5	29	57	57	90	181	181
7.5, ±2.5	119	238	238	266	532	532
7.5, ±7.5	105	209	209	238	475	475
7.5, ±12.5	76	152	152	171	342	342
7.5, ±17.5	48	95	95	105	209	209
7.5, ±22.5	21	43	43	45	90	90
7.5, ±27.5	12	24	24	19	38	38
12.5, ±2.5	43	86	86	59	119	119
12.5, ±7.5	38	76	76	57	114	114
12.5, ±12.5	33	67	67	52	105	105
12.5, ±17.5	24	48	48	40	81	81
12.5, ±22.5	14	29	29	26	52	52
12.5, ±27.5	10	19	19	19	38	38
17.5, ±2.5	19	38	38	26	52	52
17.5, ±7.5	17	33	33	26	52	52
17.5, ±12.5	12	24	24	26	52	52
17.5, ±17.5	10	19	19	26	52	52
17.5, ±22.5	7	14	14	24	48	48
17.5, ±27.5	5	10	10	19	38	38

Figure 16-2: MINIMUM INITIAL INTENSITIES

16.11.3 Maintained Minimum Intensities for Circular Indications (in cd)

	200 mm			300 mm		
Angle (v, h)	Red	Yellow	Green	Red	Yellow	Green
2.5, ±2.5	133	267	267	339	678	678
2.5, ±7.5	97	194	194	251	501	501
2.5, ±12.5	57	113	113	141	283	283
2.5, ±17.5	25	48	48	77	154	154
7.5, ±2.5	101	202	202	226	452	452
7.5, ±7.5	89	178	178	202	404	404
7.5, ±12.5	65	129	129	145	291	291
7.5, ±17.5	41	81	81	89	178	178
7.5, ±22.5	18	37	37	38	77	77
7.5, ±27.5	10	20	20	16	32	32
12.5, ±2.5	37	73	73	50	101	101
12.5, ±7.5	32	65	65	48	97	97
12.5, ±12.5	28	57	57	44	89	89
12.5, ±17.5	20	41	41	34	69	69
12.5, ±22.5	12	25	25	22	44	44
12.5, ±27.5	9	16	16	16	32	32
17.5, ±2.5	16	32	32	22	44	44
17.5, ±7.5	14	28	28	22	44	44
17.5, ±12.5	10	20	20	22	44	44
17.5, ±17.5	9	16	16	22	44	44
17.5, ±22.5	6	12	12	20	41	41
17.5, ±27.5	4	9	9	16	32	32

Figure 16-3: MAINTAINED MINIMUM INTENSITIES

16.11.4 Minimum Initial Intensities for Arrow and PV Indications (in cd/m2)

	Red	Yellow	Green
Arrow Indication	5,500	11,000	11,000
Bicycle Indication	5,500	5,500	5,500
PV Indication	future	future	future
Lane Control (X)	5,500	n/a	n/a
Lane Control (Arrow)	n/a	n/a	11,000

Figure 16-4: MINIMUM INITIAL INTENSITIES FOR ARROW AND PV INDICATIONS

16.11.5 Minimum Maintained Intensities for Arrow and PV Indications (in cd/m2)

	red	yellow	Green
Arrow Indication	5,500	11,000	11,000
Bicycle Indication	5,500	5,500	5,500
PV Indication	future	future	future
Lane Control (X)	5,500	n/a	n/a
Lane Control (Arrow)	n/a	n/a	11,000

Figure 16-5: MINIMUM MAINTAINED INTENSITIES FOR ARROW AND PV INDICATIONS

16.11.6 ~~Table 2-6~~ Chromaticity Standards (CIE Chart)

Red	Y: not greater than 0.308, or less than 0.998 - x
Yellow	Y: not less than 0.411, nor less than 0.995 - x, nor less than 0.452
Green	Y: Not less than 0.506 -.519x, nor less than 0.150 + 1.068x, nor more than 0.730 - x

Figure 16-6: CHROMATICITY STANDARDS

Section 12 FIGURES

16.12.1 Bicycle module symbol.

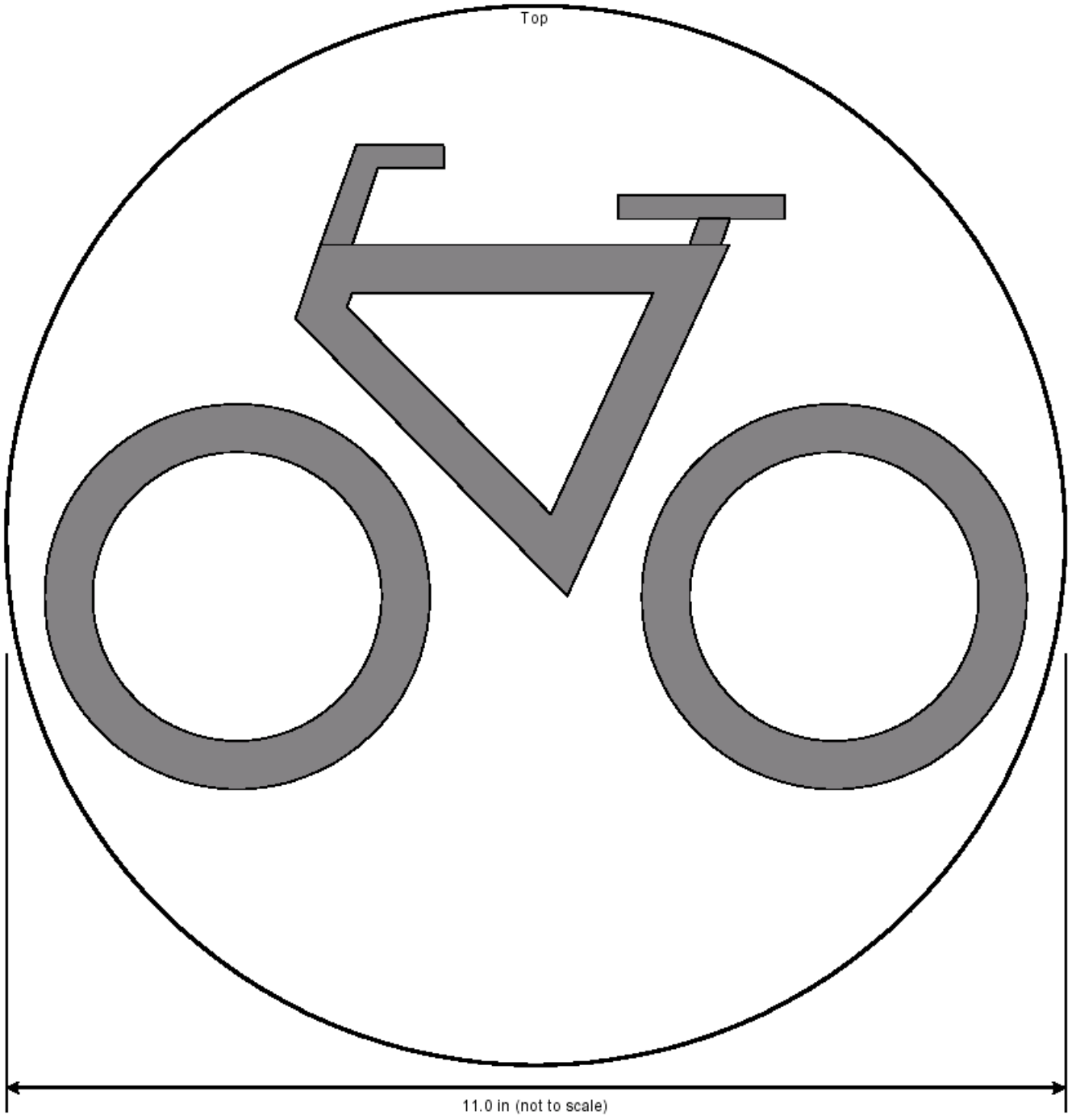


Figure 16-7: Bicycle module symbol

16.12.2 Lane Control X symbol

DRAFT *Traffic Signal*

Figure 8-1 Lane Control X symbol

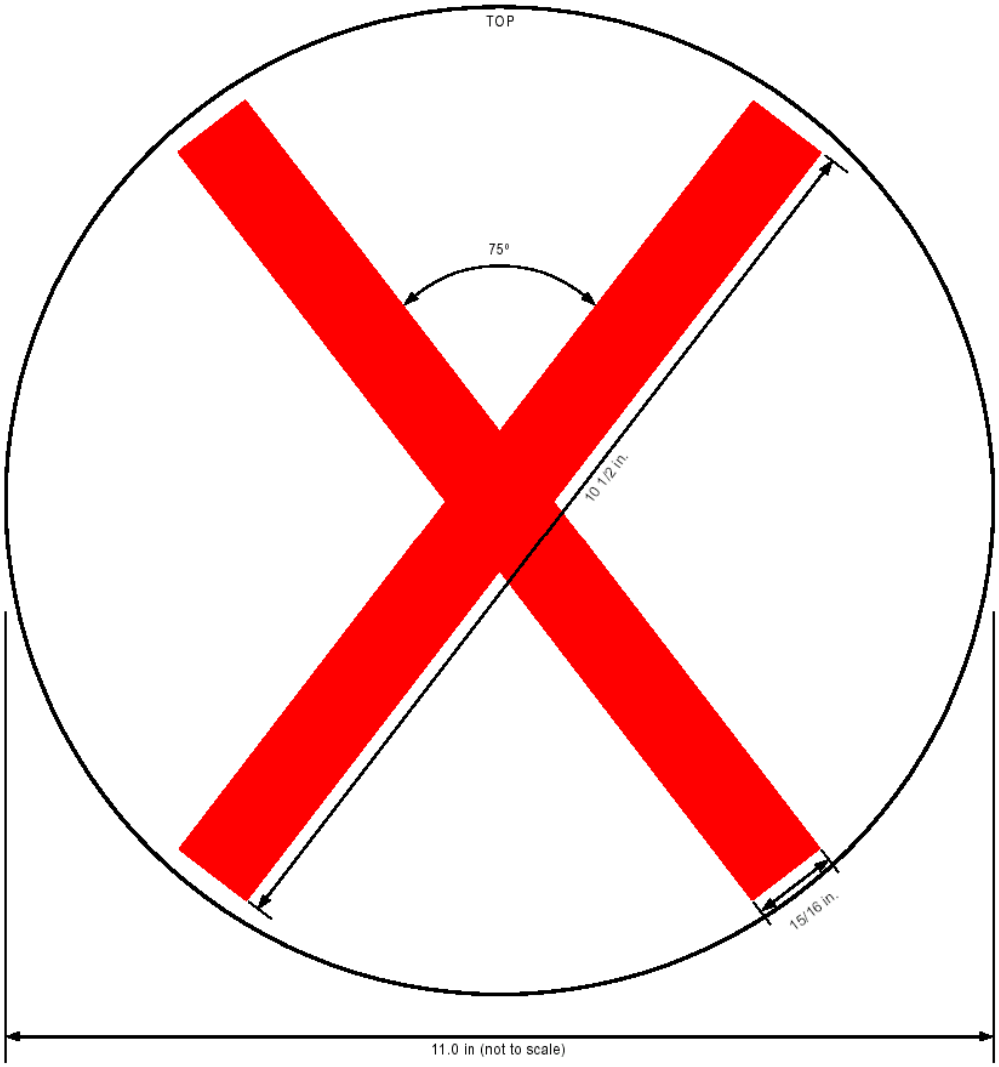


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Figure 16-8: Lane Control X symble

16.12.3 Lane Control Arrow symbol

DRAFT *Traffic Signal*

Figure 8-2 Lane Control Arrow symbol

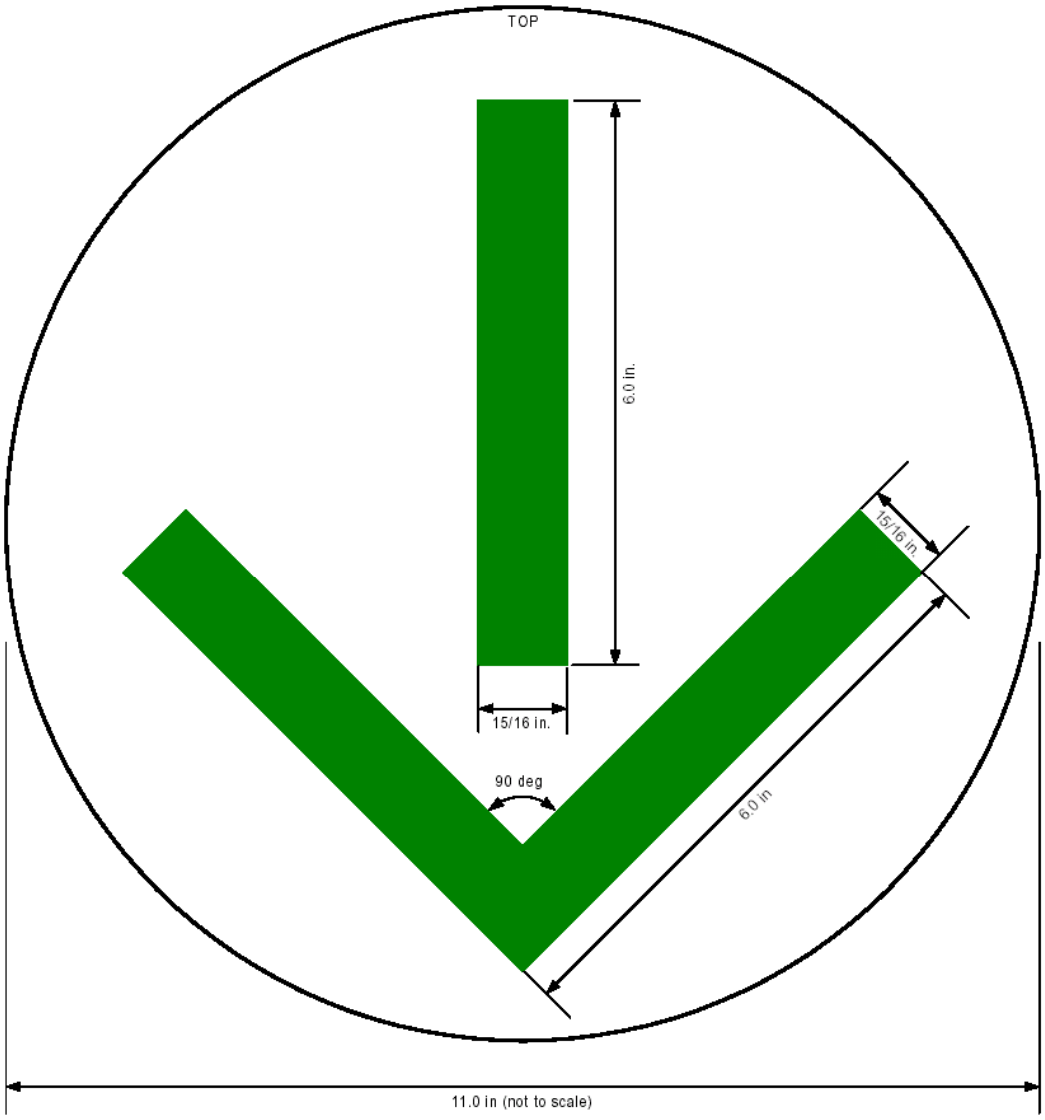

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Figure 16-9: Lane Control Arrow symbol

CHAPTER 17 LIGHT EMITTING DIODE (LED) SIGNAL MODULES (COMBINATION PEDESTRIAN SIGNAL)

Section 1 SCOPE

17.1.1 This specification is for the purchase of LED Traffic Signal Modules (herein referred to as modules) in the following configuration: Pedestrian Signal Face (Combination Signal) shall utilize light emitting diode signal modules.

17.1.2 All devices must meet the general specifications of Chapter 1--General Specifications, as well as the following specification. In case of conflict, this specification shall govern.

Section 2 GENERAL

17.2.1 Each module shall consist of an assembly that utilizes LED's as the light source in lieu of an incandescent lamp for use in traffic signal sections.

17.2.2 The LED's shall utilize appropriate technology to achieve the required color and shall be the ultra bright type rated for 100,000 hours of continuous operation from -40°C to +74°C.

17.2.3 The modules shall be rated for a minimum useful life of 48 months. All modules shall meet all parameters of this specification during this period.

17.2.4 The individual LED's shall be wired such that a catastrophic loss or the failure of one or more LED will result in the loss of not more than five percent of the signal module light output.

17.2.5 **Electrical**

17.2.5.1 Power Consumption

17.2.5.2 Maximum power consumption requirements for the modules are as follows (in Watts):

	25°C	74°C
"Hand"	10.0	12.0
"Walking Person"	9.0	12.0

17.2.5.3 LED modules will have EPA Energy Star compliance ratings, if applicable to that shape, size and color.

17.2.5.4 **Operation Voltage**

17.2.5.4.1 The modules shall operate from a 60 HZ ±3 HZ AC line over a voltage ranging from 95 volts to 135 volts. The fluctuations of line voltage shall have no visible effect on the luminous intensity of the indications.

17.2.5.4.2 Operating voltage of the modules shall be 120 VAC. All parameters shall be measured at this voltage.

17.2.5.5 **Power Factor:** The LED signal module shall have a power factor of 0.90 or greater.

17.2.5.6 **THD**: Total harmonic distortion (current and voltage) induced into an AC power line by a LED signal module shall not exceed 20 percent.

17.2.5.7 **Surge Suppression**: The signal module on-board circuitry shall include voltage surge protection to withstand high-repetition noise transients as stated in Section 2.1.6 of NEMA Standard TS-2, 1992.

17.2.5.8 The LED circuitry shall prevent perceptible flicker to the unaided eye over the voltage range specified above.

17.2.5.9 All wiring and terminal blocks shall meet the requirements of Section 13.02 of the ITE Publication: Equipment and Material Standards, Chapter 2 (Vehicle Traffic Control Signal Heads).

17.2.5.10 **Compatibility:** The modules shall be operationally compatible with currently used controller assemblies (solid state load switches, flashers, and conflict monitors). Review CHAPTER 2, CHAPTER 3, CHAPTER 4, CHAPTER 5, CHAPTER 9 and CHAPTER 1 for specifications on these devices.

17.2.5.11 When a current of 20 mA AC (or less) is applied to the unit, the voltage read across the two leads shall be 15 VAC or less.

17.2.5.12 The modules and associated on-board circuitry must meet Class A emission limits referred in Federal Communications Commission (FCC) Title 47, SubPart B, Section 15 regulations concerning the emission of electronic noise.

17.2.6 **Environmental Requirements**

17.2.6.1 The LED signal module shall be rated for use in the operating temperature range of -40°C (-40°F) to +74°C (+165°F). The modules shall meet all specifications throughout this range.

17.2.6.2 The LED signal module shall be protected against dust and moisture intrusion per the requirements of NEMA Standard 250-1991 for Type 4 enclosures to protect all internal components.

17.2.7 **Construction**

17.2.7.1 The LED signal module shall be a single, self-contained device, not requiring on-site assembly for installation into an existing traffic signal housing. The power supply for the module shall be integral to the unit.

17.2.7.2 The circuit board and power supply shall be contained inside the module. Circuit boards shall conform to Chapter 1, Section 6 of the "Transportation Electrical Equipment Specifications".

17.2.7.3 The assembly and manufacturing process for the LED signal assembly shall be designed to assure all internal components are adequately supported to withstand mechanical shock and vibration from high winds and other sources.

17.2.8 **Materials**

17.2.8.1 Material used for the lens and signal module construction shall conform to ASTM specifications for the materials.

17.2.8.2 Enclosures containing either the power supply or electronic components of the signal module shall be made of UL94VO flame retardant materials. The lens of the signal module is excluded from this requirement.

17.2.9 **Module Identification**

17.2.9.1 Each module shall have the manufacturer's name, trademark, model number, serial number, date of manufacture (month-year), and lot number as identification permanently marked on the back of the module.

17.2.9.2 The following operating characteristics shall be permanently marked on the back of the module: rated voltage and rated power in Watts and Volt-Ampere.

17.2.9.3 If a specific mounting orientation is required, each module shall have prominent and permanent marking(s) for correct indexing and orientation within a signal housing. The markings shall consist of an up arrow, or **the word "UP" or "TOP".**

Section 3 TYPE A PEDESTRIAN SIGNAL FACE (COMBINATION RAISED HAND/WALKING PERSON SECTION)

17.3.1 **Scope:** The following specifications requirements apply to the Walking Person section only. All general specifications apply unless specifically superceded in this section.

17.3.2 **General**

17.3.2.1 Pedestrian signal face modules shall be designed to mount behind or replace the existing face plate of existing Type "A" housing as specified by the requirements in the ITE Publication: Equipment and Material Standards, Chapter 3 (Pedestrian Traffic Control Signal Indications).

17.3.2.2 The design of the modules shall require a specific mounting orientation.

17.3.3 **Photometric Requirements**

17.3.3.1 Each module shall provide an average luminous intensity of at least 3,750 candela/m2 for "Hand" and 5,300 candela/m2 for "Walking Person" symbol throughout the useful life over the operating temperature range.

17.3.3.2 The uniformity ratio of an illuminated symbol shall not exceed 4 to 1, between the highest luminance area and the lowest luminance area in the module.

17.3.3.3 The color output of the module shall conform to the requirements of Section 5.3 in the ITE Publication: Equipment and Material Standards, Chapter 3 (Pedestrian Traffic Control Signal Indications).

17.3.3.4 "Hand" shall be Portland orange. not greater than 0.390, nor less than 0.331, nor less than 0.997 - x

17.3.3.5 Walking person shall be lunar white.

x: not less than 0.290 nor greater than 0.330
y: not less than 1.5x – 0.175 nor greater than 1.5x – 0.130

17.3.4 **Physical and Mechanical Requirements**

17.3.4.1 The module shall be designed to be used in the pedestrian signal section as retrofit replacement for existing signal lamps and shall not require special tools for installation.

17.3.4.2 The module shall fit into existing pedestrian signal section housings built to the PTCSH specifications without modification to the housing.

17.3.4.3 The height of each symbol on the module shall be not less than 250 mm and the width of each symbol on the module shall not be less than 165 mm.

17.3.4.4 **Construction:** The modules shall be a single, self-contained device, not requiring on-site assembly for installation into an existing Type "A" housing.

Section 4 QUALITY ASSURANCE

17.4.1 The modules shall be manufactured in accordance with a manufacturer quality assurance (QA) program. The QA program shall include two types of quality assurance: (1) design quality assurance and (2) production quality assurance. The production quality assurance shall include statistically controlled routine tests to ensure minimum performance levels of LED signal modules built to meet this specification, and a documented process of how problems are to be resolved.

17.4.2 QA process and test results documentation shall be kept on file for a minimum period of seven years.

17.4.3 LED signal module designs not satisfying design qualification testing and the production quality 4.3 assurance testing performance requirements described below shall not be labeled, advertised, or sold as conforming to this specification.

17.4.4 **Design Qualification Testing**

17.4.4.1 Design Qualification Testing shall be performed by the manufacturer or an independent testing lab hired by the manufacturer on new LED module designs, and when a major design change has been implemented on an existing design.

17.4.4.2 A major design change is defined as a design change (electrical or physical) which changes any of the performance characteristics of the module, results in a different circuit configuration for the power supply, or changes the layout of the individual LED's in the module.

17.4.4.3 A quantity of two units for each design shall be submitted for Design Qualification Testing.

17.4.4.4 Test units shall be submitted to Caltrans Laboratory, Electrical Testing Branch, after the manufacturer's testing is complete.

17.4.4.5 Manufacturer's testing data shall be submitted with test units for Caltrans verification of Design Qualification Testing data.

17.4.4.6 **Burn-In:** The sample modules shall be energized for a minimum of 24 hours, at 100 percent on-time duty cycle, at a temperature of +74°C (+165°F), before performing any design qualification testing.

17.4.4.7 Any failure of the module, which renders the unit non-compliant with the specification after burn-in, shall be cause for rejection.

17.4.4.8 For Design Qualification Testing, all specifications will be measured including, but not limited to:

17.4.4.8.1 Rated Initial Luminous Intensity, measured over the operating temperature range.

17.4.4.8.2 Chromaticity (Color), measured over the operating temperature range.

17.4.4.8.3 Electrical. All specified parameters shall be measured and used for quality comparison of production quality assurance on production modules (rated power, etc).

17.4.4.8.4 Equipment Compatibility. Modules shall be tested for compatibility with the controller unit, conflict monitor, and load switch. Each signal module shall be connected to the output of a standard load switch, connected to an AC voltage supply between the values of 95 and 135 VAC, with the input to the load switch in the "off" position. The AC voltage developed across each LED signal module so connected shall not exceed 10 Vrms as the input AC voltage is varied from 95 Vrms to 135 Vrms.

17.4.4.8.5 Mechanical vibration testing shall be as per MIL-STD-883, Test Method 2007, using 3 four minute cycles along each x, y, and z axis, at a force of 2.5 Gs, with a frequency sweep from 2 HZ to 120 HZ. The loosening of the lens, or of any internal components, or other physical damage shall be cause for rejection.

17.4.4.8.6 Temperature cycling shall be performed as per MIL-STD-883, Test method 1010. The temperature range shall be per "Environmental Requirements". A minimum of 20 cycles shall be performed with a 30 minute transfer time between temperature extremes and a 30 minute dwell time at each temperature. Module (s) being tested shall be energized and functioning throughout the duration of the test. Failure of a module to function properly or any evidence of cracking of the module lens or housing after temperature cycling shall be cause for rejection.

17.4.4.8.7 Moisture resistance testing shall be performed on all modules mounted in a standard type "A" pedestrian housing per NEMA Standard 250-1991 for Type 4 enclosures. Any evidence of internal moisture after testing shall be cause for rejection.

17.4.5 **Production Quality Control Testing.**

17.4.5.1 The following Production Quality Assurance tests shall be performed on each new module prior to shipment. Failure to meet requirements of any of these tests shall be cause for rejection. Test results shall be retained by the manufacturer for seven years.

17.4.5.2 Burn-in period shall consist of each signal module being energized at rated voltage for a 30-minute stabilization period before the measurement is made.

17.4.5.3 Each module shall be tested for rated initial intensity after burn-in.

17.4.5.4 A single point measurement, with a correlation to the intensity requirements of Section 1.04 of the VTCSH for circular modules, may be used.

17.4.5.5 The ambient temperature for this measurement shall be +25°C (+77°F).

17.4.5.6 Each module not meeting minimum luminous intensity requirements of 3,750 cd/m2 for Hand and 5300 cd/m2 for Walking Person Symbol shall be cause for rejection.

17.4.5.7 Each module shall be tested for required power factor after burn-in.

17.4.5.8 Each module shall be measured for current flow in amperes after burn-in. The measured current values shall be compared against rated values resulting from design qualification measurements under "Design Qualification Testing". The current flow shall not exceed the rated value.

17.4.5.9 Each module shall be visually inspected for any exterior physical damage or assembly anomalies. Careful attention shall be paid to the surface of the lens to ensure there are no scratches (abrasions), cracks, chips, discoloration, or other defects. Any such defect shall be cause for rejection.

17.4.6 **County Quality Assurance Testing**.

17.4.7 The County may perform testing on all shipments.

17.4.8 Testing should be completed within 30 days after delivery to the specified location on the purchase order.

17.4.9 All parameters of the specification may be tested.

17.4.10 Acceptance/Rejection of the shipment shall at the County's.

17.4.11 **Warranty**

17.4.12 The manufacturer shall provide a written warranty against defects in materials and workmanship for the modules for a minimum period of 60 months after acceptance of the modules. Replacement modules shall be provided promptly after receipt of modules that have failed at no cost to the State. All warranty documentation shall be given to the TransLab prior to random sample testing.

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